Model Name: GA-Z68XP-UD4 1.0

SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS*16/*8 SWITCH
17	PCI EXPRESS*1 SLOTs X3
18	PI7C9X113SL
19	PI7C9X113SL POWER
20	PCI SLOT 1&2
21	I/O ITE8728
22	COM, -PROHOT, ESATA CONNECT
23	Dual BIOS , TPM SLB9635TT
24	ALC892
25	REAR AUDIO JACK
26	VCORE PWM_ISL6366CRZ-1
27	VCORE PWM_ISL6366CRZ-2

SHEET	TITLE
28	VCORE PWM_ISL6366CRZ-3
29	DISCRETE POWER I
30	DDR_15V & VCC1_05_PCH PWM_ISL6545CBZ
31	CPU_VTT PWM_ISL6322G
32	VCCSA POWER
33	F_PANEL , F_USB , FDD
34	ATX POWER, CLOCK GEN
35	HWM,KB/MS , FAN CTRL
36	REALTEK RTL8111E
37	ESATA SE9128
38	FRONT NEC USB3.0
39	REAR NEC USB3.0
40	TABLE LIST

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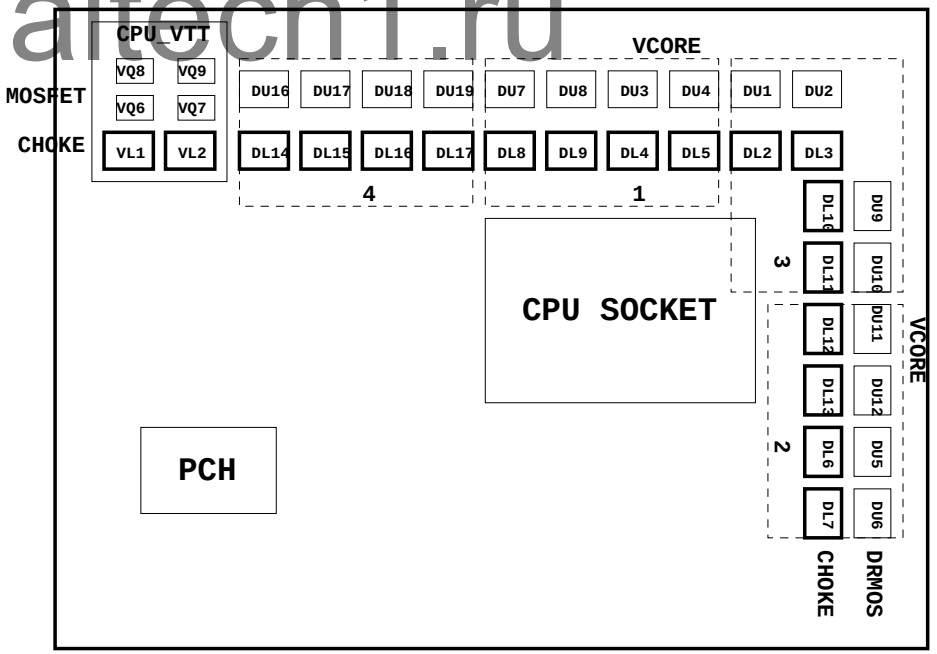

Gigabyte Technology

Title: Cover Sheet

Size: Custom | Document Number: GA-Z68XP-UD4 | Rev: 1.0

Date: Thursday, May 19, 2011 | Sheet 1 of 44

GA-Z68XP-UD4

Component value change history

Data	Change Item	Reason
2011/04/14	1.0A-EBOM	
	Modify from Z68X-UD4-B3-1.01G PBOM	
2011/05/16	1.0B-PBOM	

Circuit or PCB layout change

DATE	Change Item	Reason
1.0A 2011/04/14	1. Modify from Z68X-UD4-B3 1.01 2. Add 1 phase Vaxg power 3. remove turbo USB3	
1.0B 2011/05/16	1. Modify from Z68XP-UD4 1.0A 2. Modify VAXG Loadline & ttransient: DR409 10KΩ → 8.66kΩ DR411 680Ω → 340Ω DC159 47P → 82P DR392 4.99KΩ → 32.4KΩ DR396 499Ω → 2.8KΩ DR399 1.1KΩ → 499Ω DR397 Remove	
1.0B 2011/05/17	1. Modify VAXG Loadline DR396 2.8kΩ → 1.18KΩ DR392 32.4KΩ→16.9k	

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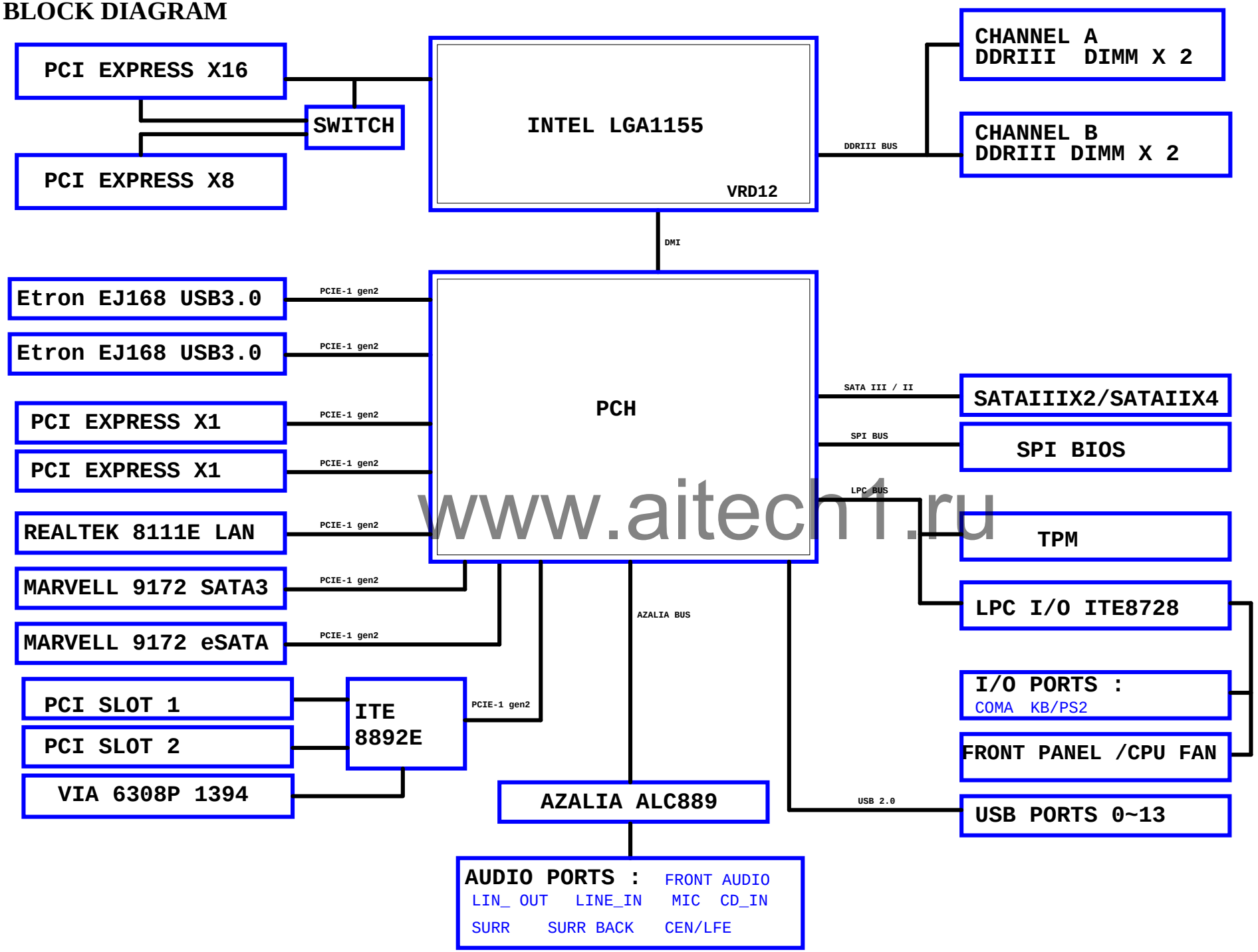
Title: BOM & PCB MODIFY HISTORY

Size: Custom | Document Number: GA-Z68XP-UD4 | Rev: 1.0

Date: Thursday, May 19, 2011 | Sheet 2 of 44

BLOCK DIAGRAM



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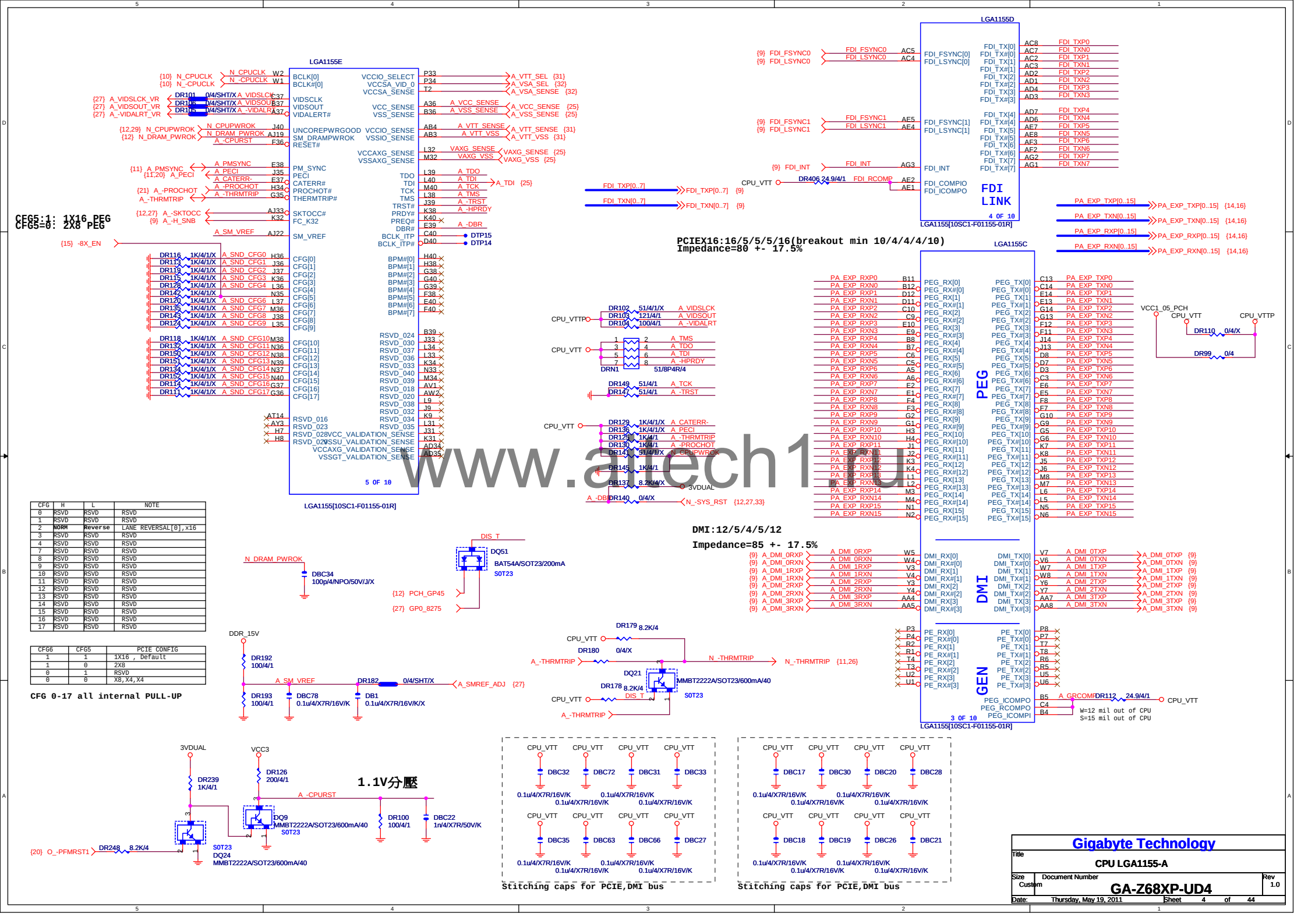
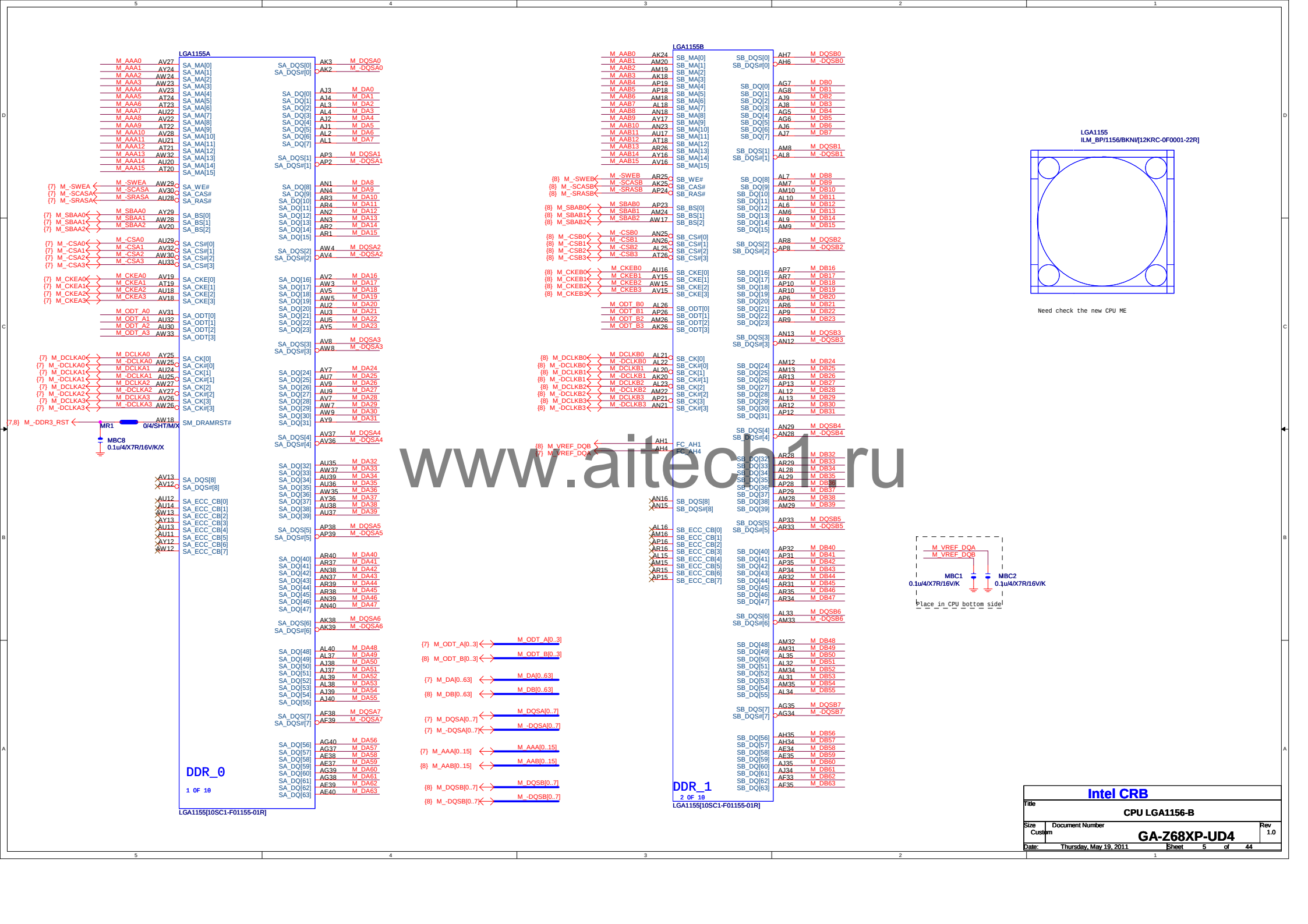
Gigabyte Technology			
Title: BLOCK DIAGRAM			
Size: C	Document Number: GA-Z68XP-UD4		Rev: 1.0
Date: Thursday, May 19, 2011	Sheet 3 of 44		



CFG	H	L	NOTE
0	RSVD	RSVD	RSVD
1	RSVD	RSVD	RSVD
2	NORM	Reverse	LANE REVERSAL[0],x16
3	RSVD	RSVD	RSVD
4	RSVD	RSVD	RSVD
7	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD
11	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD
14	RSVD	RSVD	RSVD
15	RSVD	RSVD	RSVD
16	RSVD	RSVD	RSVD
17	RSVD	RSVD	RSVD

CFG6	CFG5	PCIE CONFIG
1	1	1X16 , Default
1	0	2X8
0	1	RSVD
0	0	X8,X4,X4

Gigabyte Technology		
Title	CPU LGA1155-A	
Size: Custom	Document Number: GA-Z68XP-UD4	Rev: 1.0
Date: Thursday, May 19, 2011	Sheet 4 of 44	



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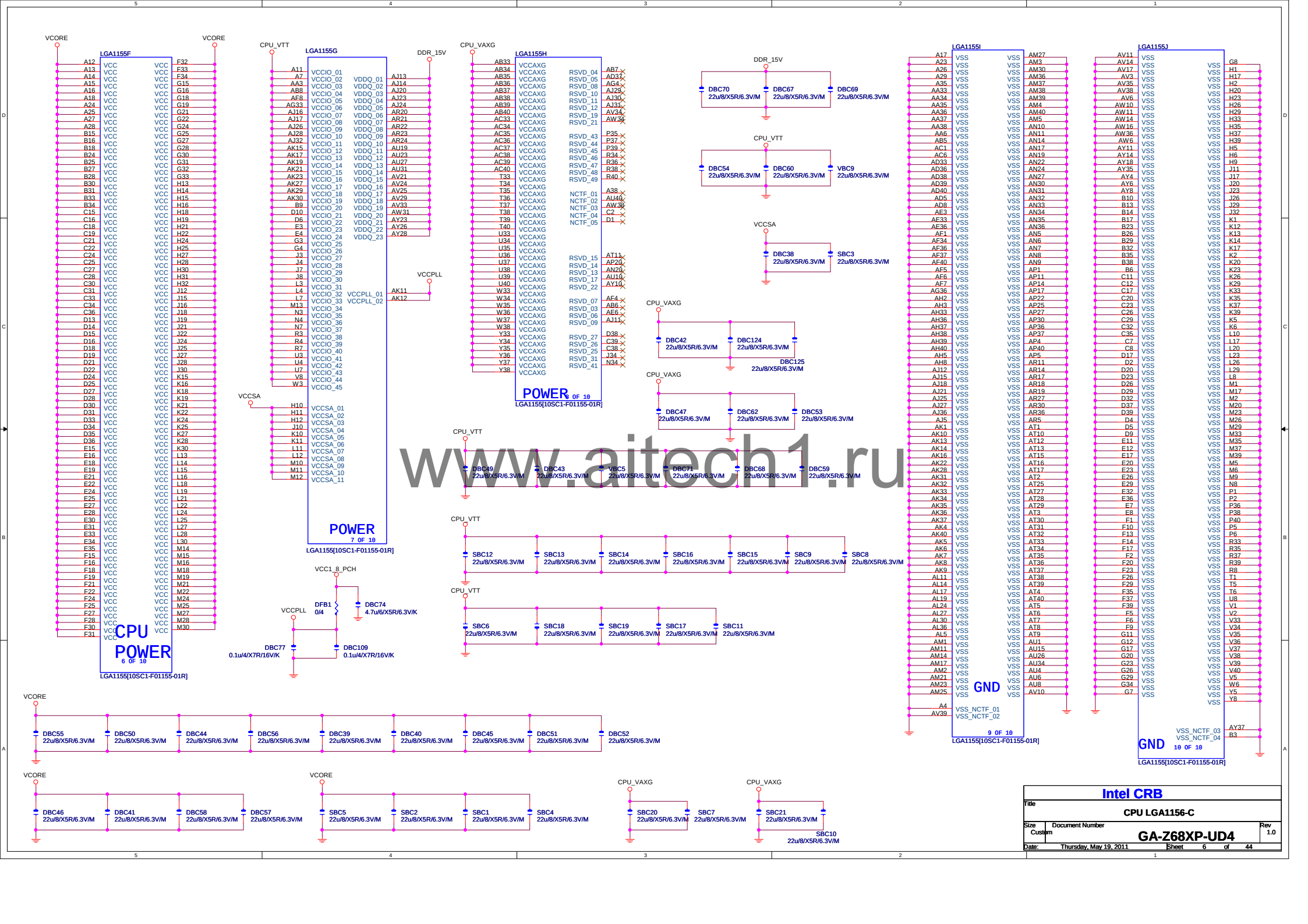

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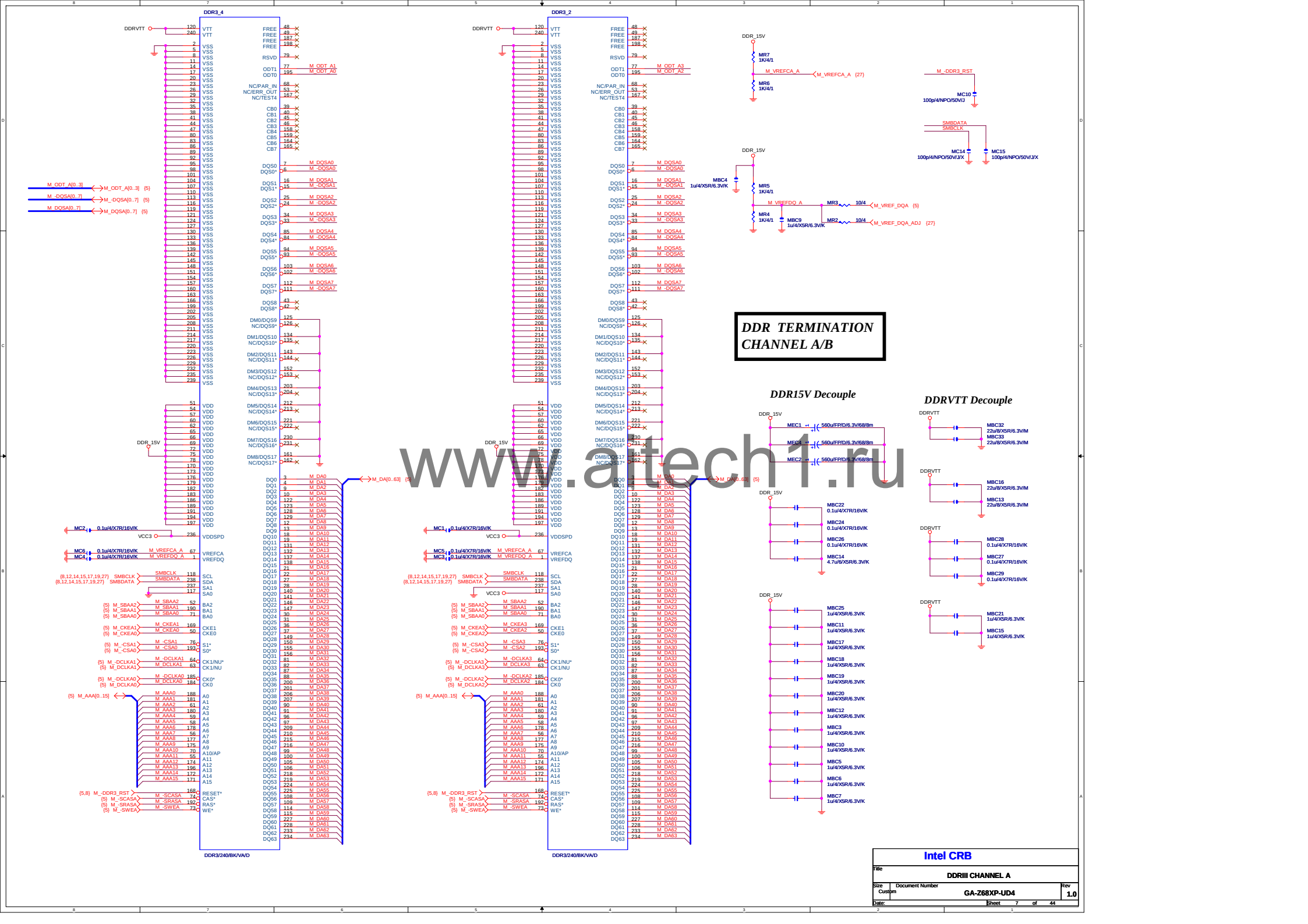
Intel CRB		
Title	CPU LGA1156-C	
Size: Custom	Document Number: GA-Z68XP-UD4	Rev: 1.0
Date: Thursday, May 19, 2011	Sheet 6 of 44	



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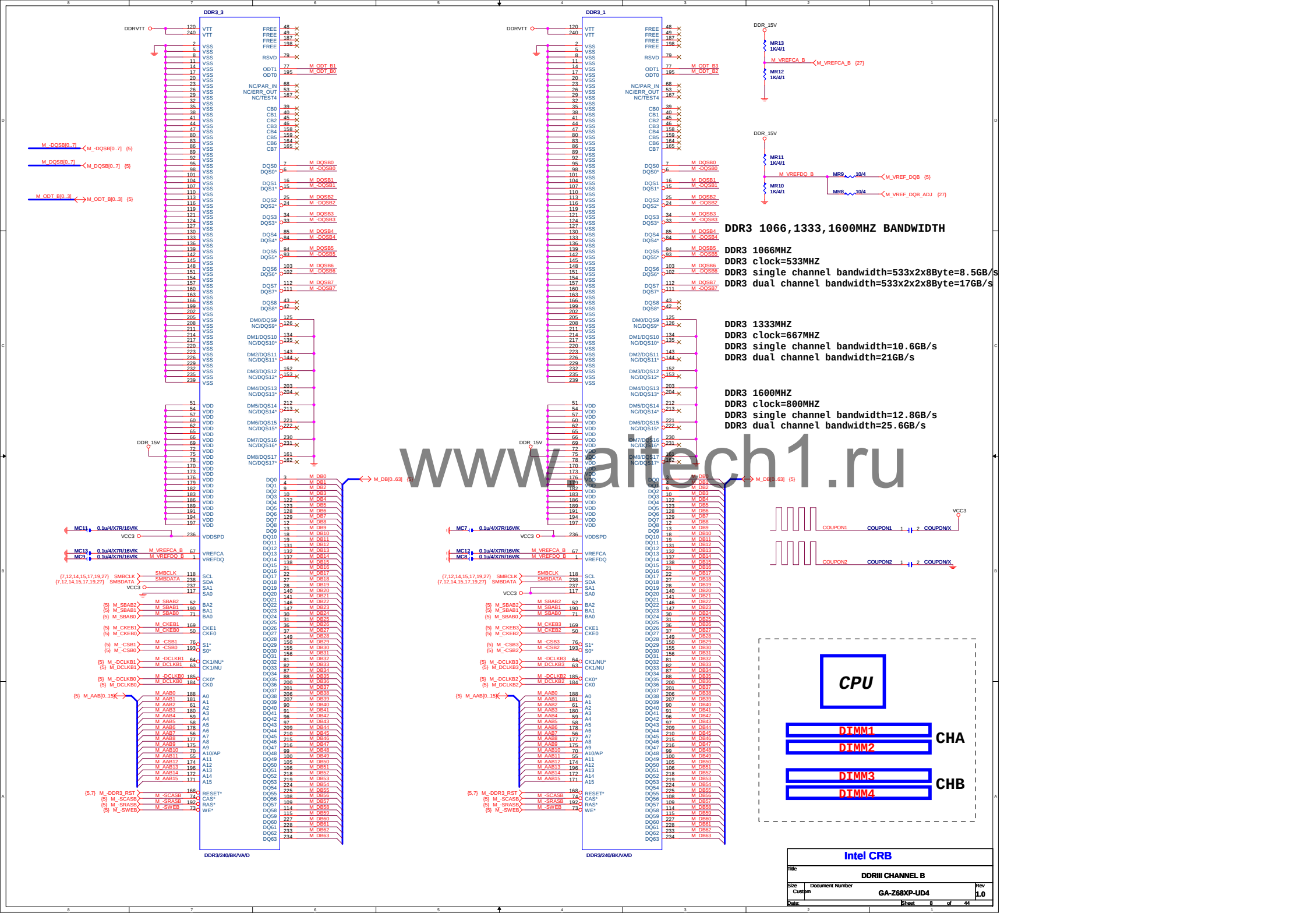

DDR3 1066,1333,1600MHZ BANDWIDTH

DDR3 1066MHZ
DDR3 clock=533MHZ
DDR3 single channel bandwidth=533x2x8Byte=8.5GB/s
DDR3 dual channel bandwidth=533x2x2x8Byte=17GB/s

DDR3 1333MHZ
DDR3 clock=667MHZ
DDR3 single channel bandwidth=10.6GB/s
DDR3 dual channel bandwidth=21GB/s

DDR3 1600MHZ
DDR3 clock=800MHZ
DDR3 single channel bandwidth=12.8GB/s
DDR3 dual channel bandwidth=25.6GB/s

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Intel CRB

Title: DDRIII CHANNEL B

Size: Custom | Document Number: GA-Z68XP-UD4 | Rev: 1.0

Date: | Sheet 8 of 44

USB:12/7.5/4.5/7.5/12 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%

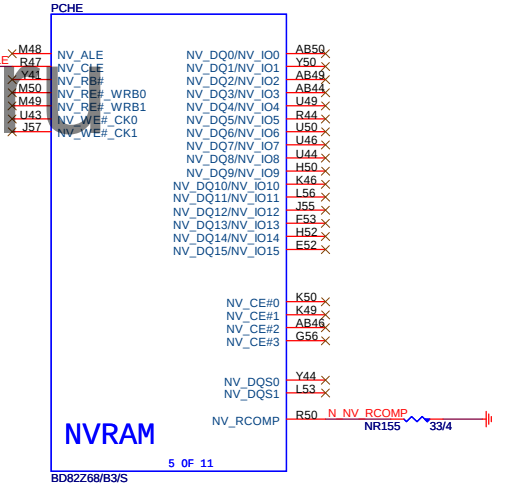
OC[3:0]# for Device 29 (ports 0-7)

OC[7:4]# for Device 26 (ports 8-13)

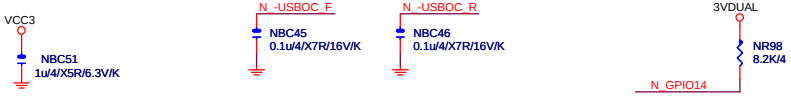
USB OC# Configure	
OC0#	USB0,1
OC1#	USB2,3
OC2#	USB4,5
OC3#	USB6,7
OC4#	USB8,9
OC5#	USB10,11
OC6#	USB12,13
OC7#	Not Use

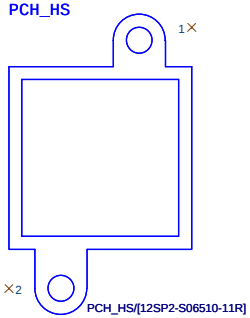
FDI_TXP[0..7] → FDI_TXP[0..7] {4}

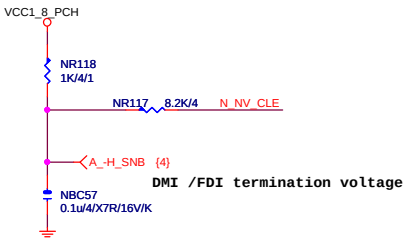
FDI_TXN[0..7] → FDI_TXN[0..7] {4}



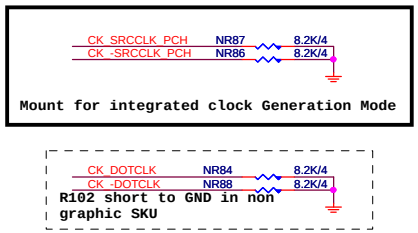
PCIEX1:16/5/5/5/16 (breakout min 8/4/4/4/8)
Impedance=80 +- 17.5%







DMI /FDI termination voltage



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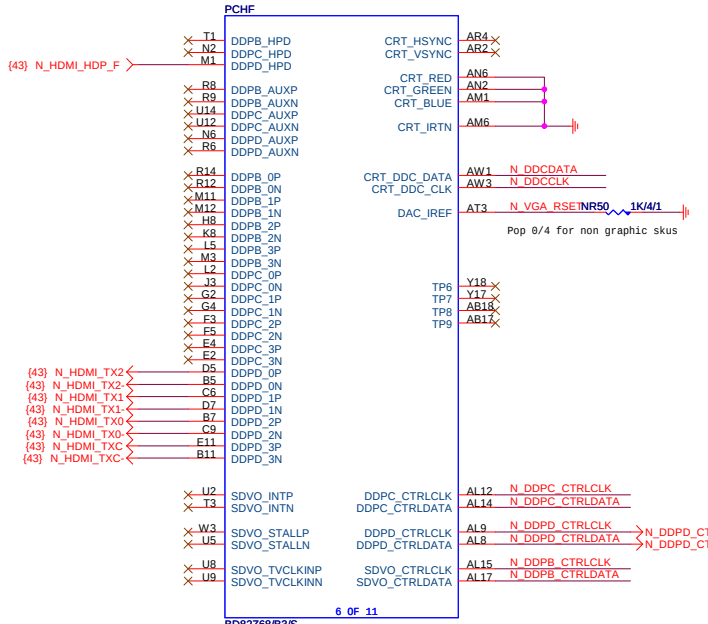
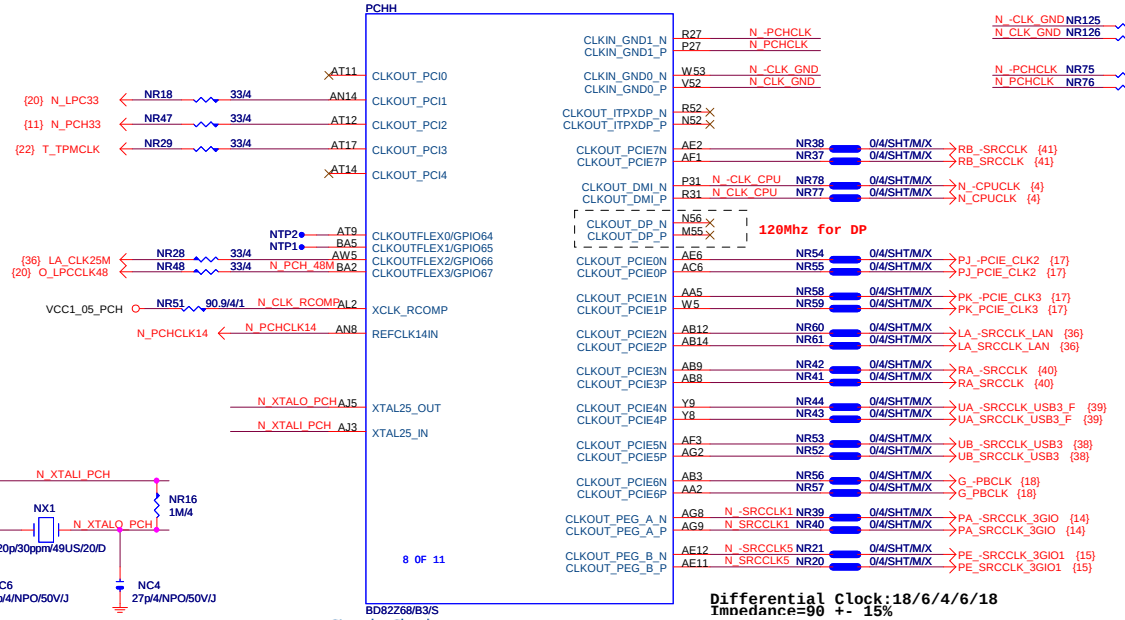
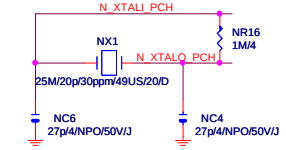
Gigabyte Technology			
Title: PCH FDI,DMI,USB ,PCIE			
Size: Custom	Document Number: GA-Z68XP-UD4		Rev: 1.0
Date: Thursday, May 19, 2011		Sheet 9 of 44	

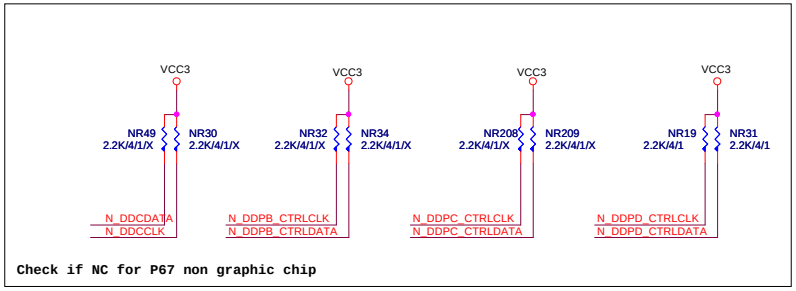


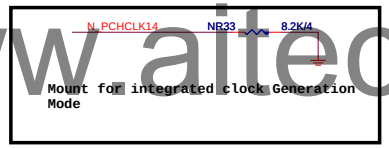
Flex0,2 : 33MHZ

Flex1,3 : 27/14/24/48/25MHZ









Strapping Signals

Name	Type	Recommendations	Reason/Impact
SPKR	I	**Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2k-10k Ohm weak pull-up resistor.	
INIT3_3V#	I	Do not pull low.	
GNT3#/ GPIO55	I/O	**Default Mode:** Internal pull-up. **Top Block Swap Mode:** Connect to ground with 4.7k Ohm weak pull-down resistor.	
SATA1GP/ GPIO19, GNT1#	I/O	**Default (SPI)** Left both SATA1GP/GPIO19 and GNT1# floating. No pull up required. **Boot from PCI** Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor. Leave GNT1# Floating. **Boot from LPC** Connect both SATA1GP/GPIO19 and GNT1# to ground with 1k Ohm pull-down resistor.	If LPC is selected BIOS may still be placed on LPC, but all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.
GNT2#/ GPIO53	I/O	Do not pull low.	ESI strap for server platform ONLY
HDA_SDO	I/O	**Default** Do not pull high. **Disable ME in Manufacturing Mode** Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.	Flash descriptor Overide
SPI_MOSI	I/O	Internal weak pull down.Do not pull high.	DMI RX Termination Voltage
DF_TVS	I/O	Internal weak pull up. Do not pull low.	DMI termination voltage
HDA_SYNC	I/O	Internal weak pull down. Do not pull up.	On die PLL VR volatge selector
GPIO15	I/O	**Enable TLS:** Pull up with 1k Ohm to VccSus3.3. **Default (Disable TLS):** Leave NC. Internal pull down.	TLS confidentiality
GPIO8	I/O	**BTM** Leave floating. Do not pull low. **FCIM** Pull low with 1k Ohm to ground.	FCIM. Can be override by softstrap through ME.
GPIO28	I/O	Internal weak pull up. Do not pull low.	On die PLL voltage regulator
SATA2GP/ GPIO36	I/O	Internal weak pull down.Do not pull high.	
SATA3GP/ GPIO37	I/O	Internal weak pull down.Do not pull high.	

Differential Clock:18/6/4/6/18
Impedance=90 +- 15%

GP29 , 35, 36 , 37 power on with 3.3V pluse

GP8 always Hi without PU

GP20 with pluse during power on & reset

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Title: PCH DISPLAY ,CLK BUFFER

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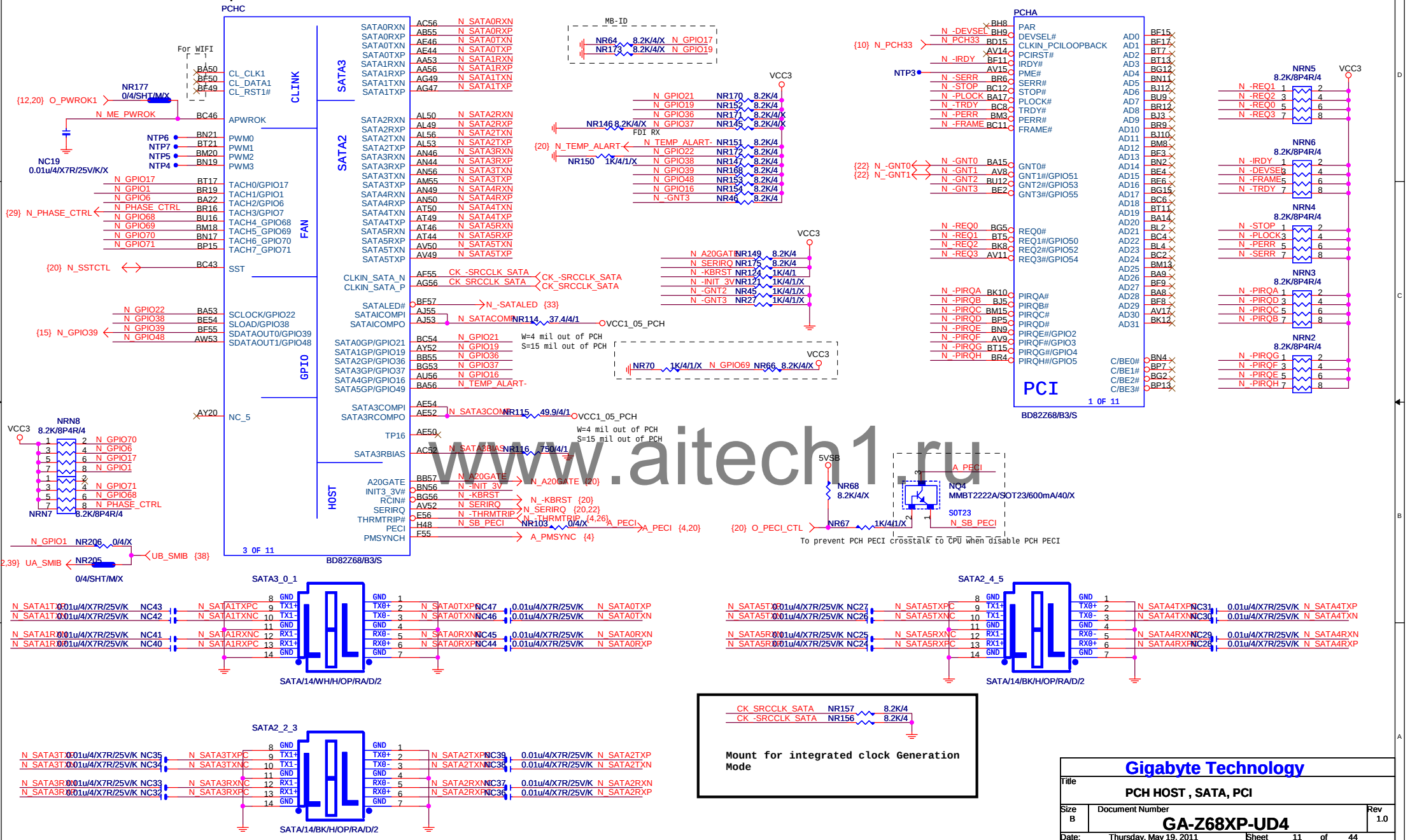
SATA:20/7.5/4.5/7.5/20 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%



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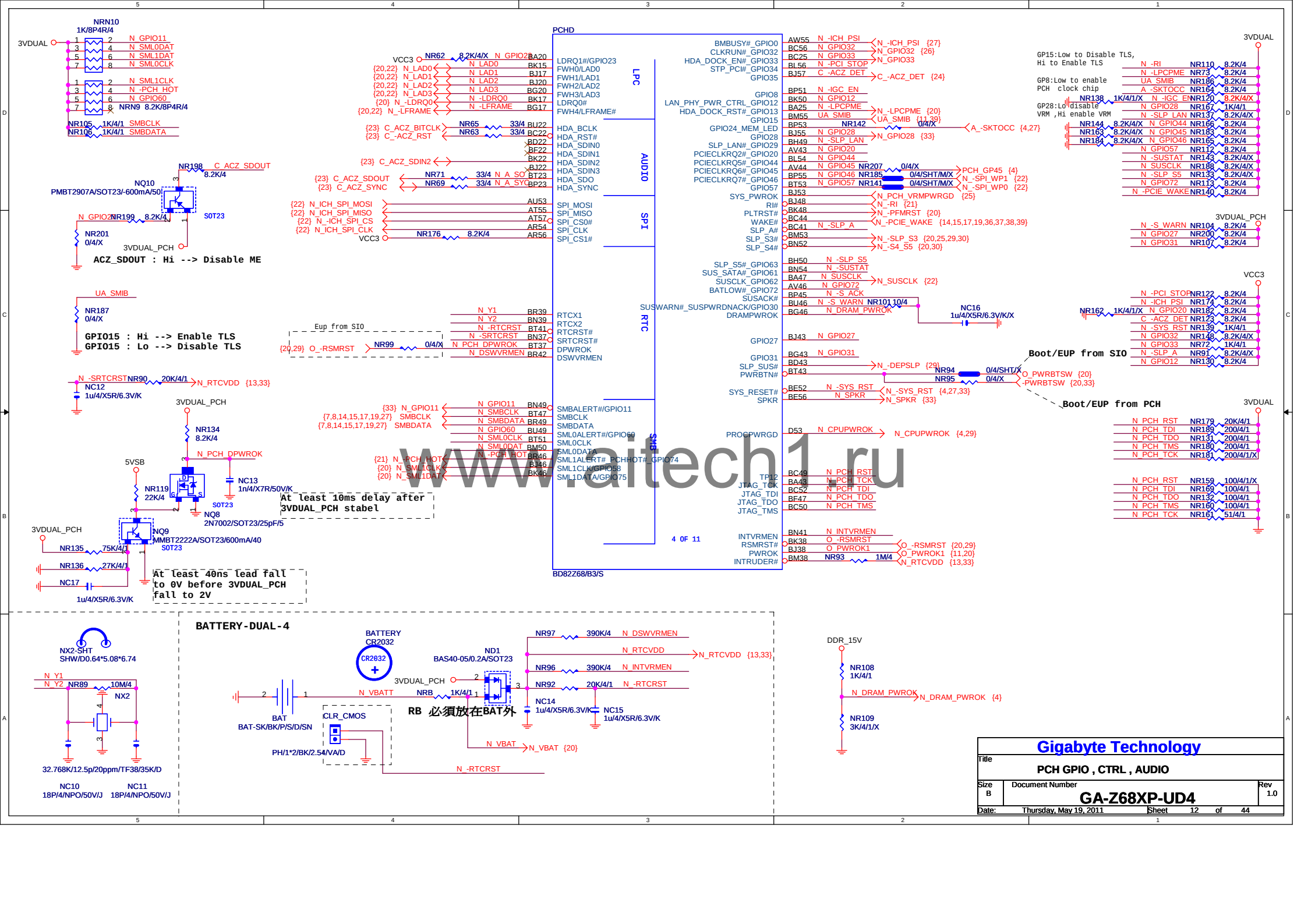
Gigabyte Technology	
Title	PCH HOST , SATA, PCI
Size B	Document Number GA-Z68XP-UD4 Rev 1.0
Date: Thursday, May 19, 2011	Sheet 11 of 44



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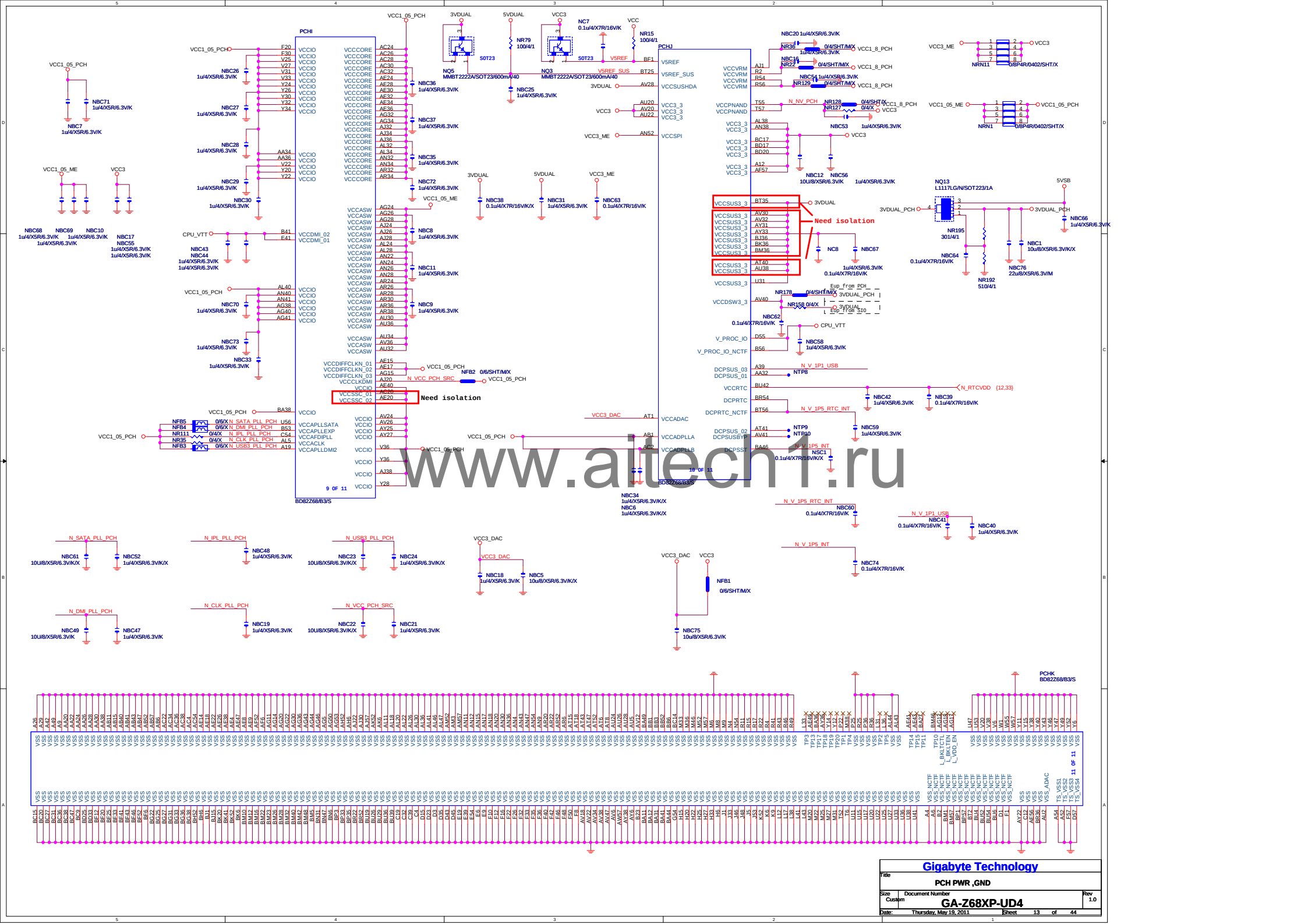

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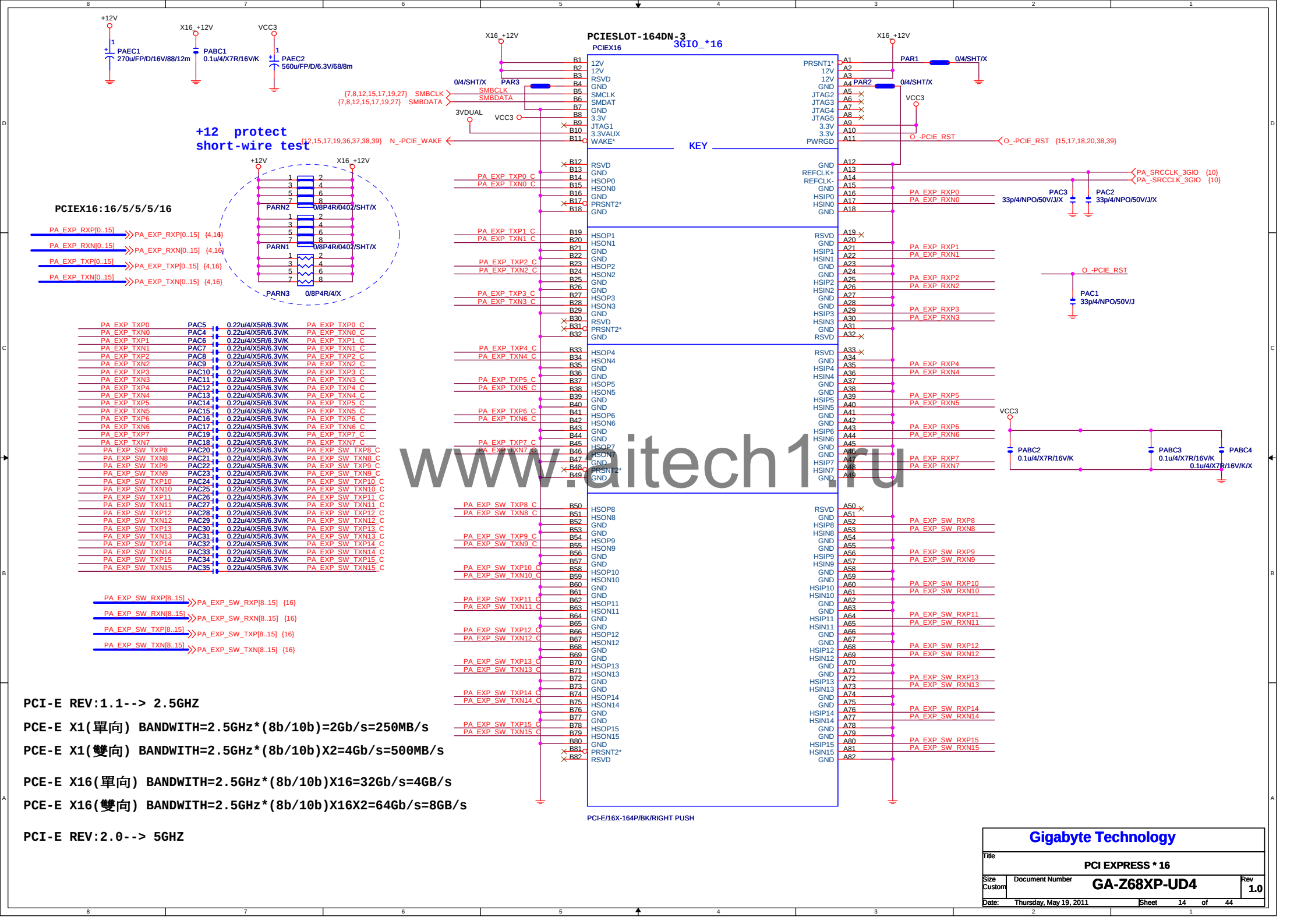

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PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

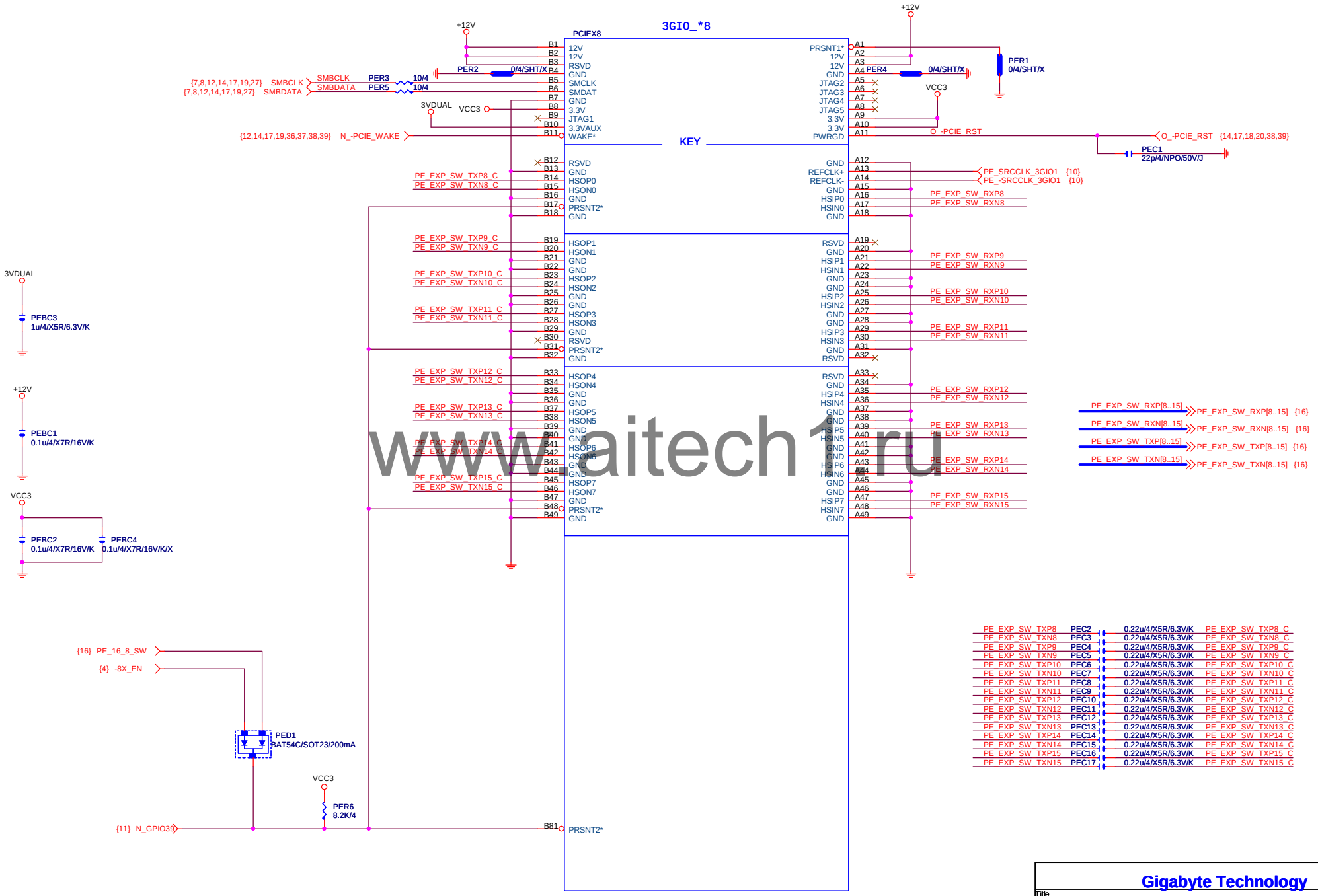
PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

Gigabyte Technology	
Title	PCI EXPRESS * 16
Size: Custom	Document Number: GA-Z68XP-UD4
Rev: 1.0	
Date: Thursday, May 19, 2011	Sheet 14 of 44



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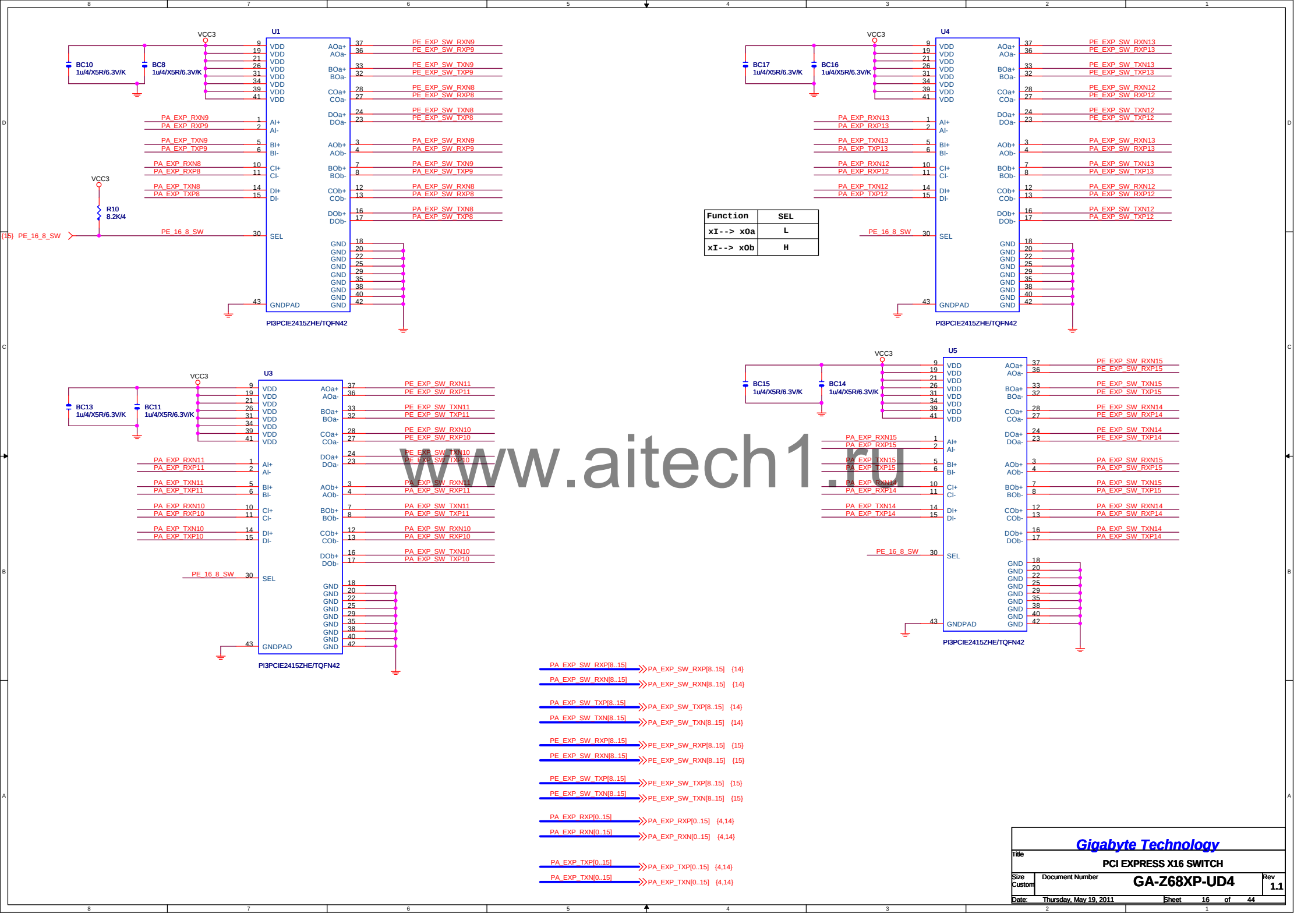
Title	PCI EXPRESS X 4 PORT
Size	Custom
Document Number	GA-Z68XP-UD4
Rev	1.0
Date:	Thursday, May 19, 2011
Sheet	15 of 44

Gigabyte Technology



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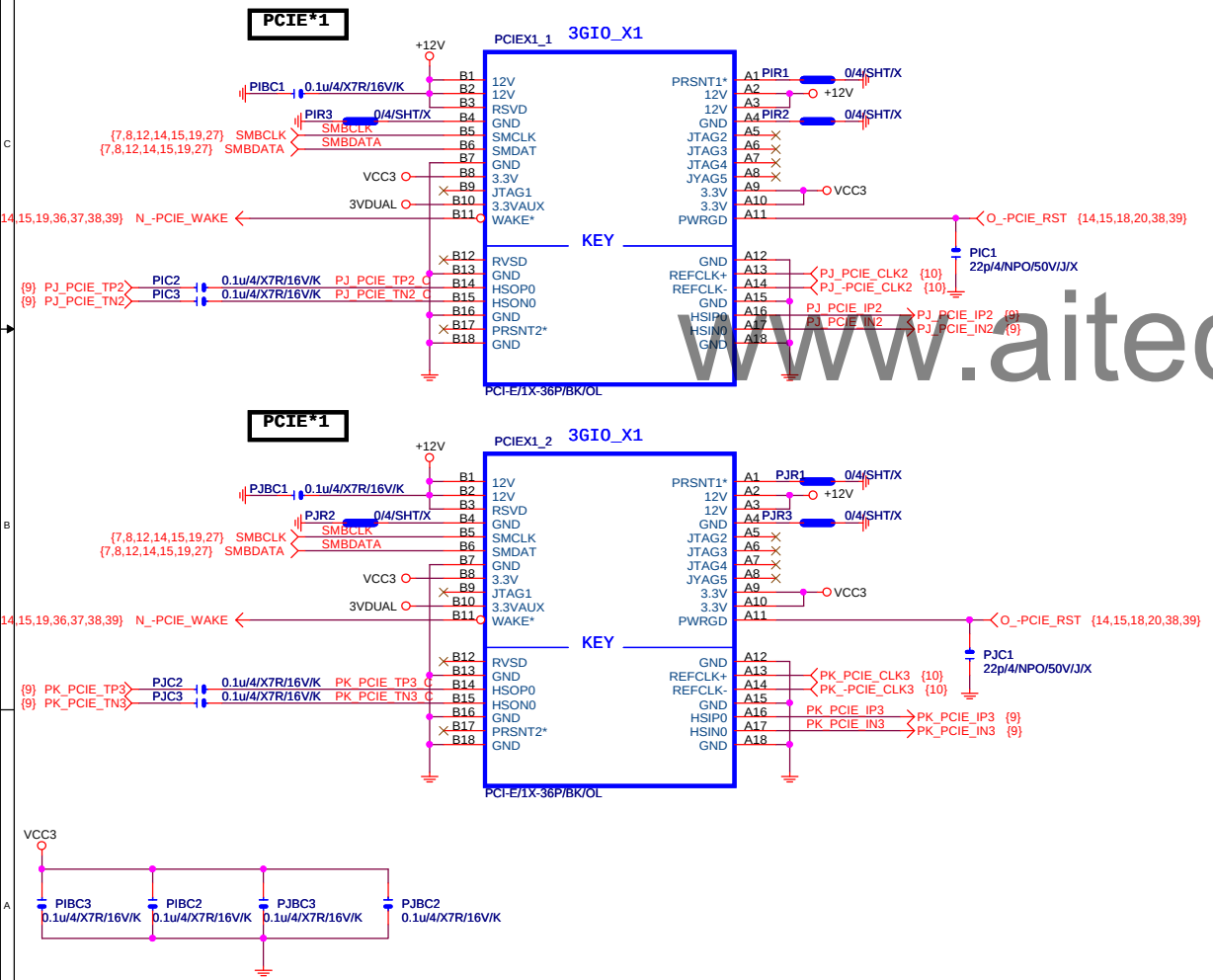

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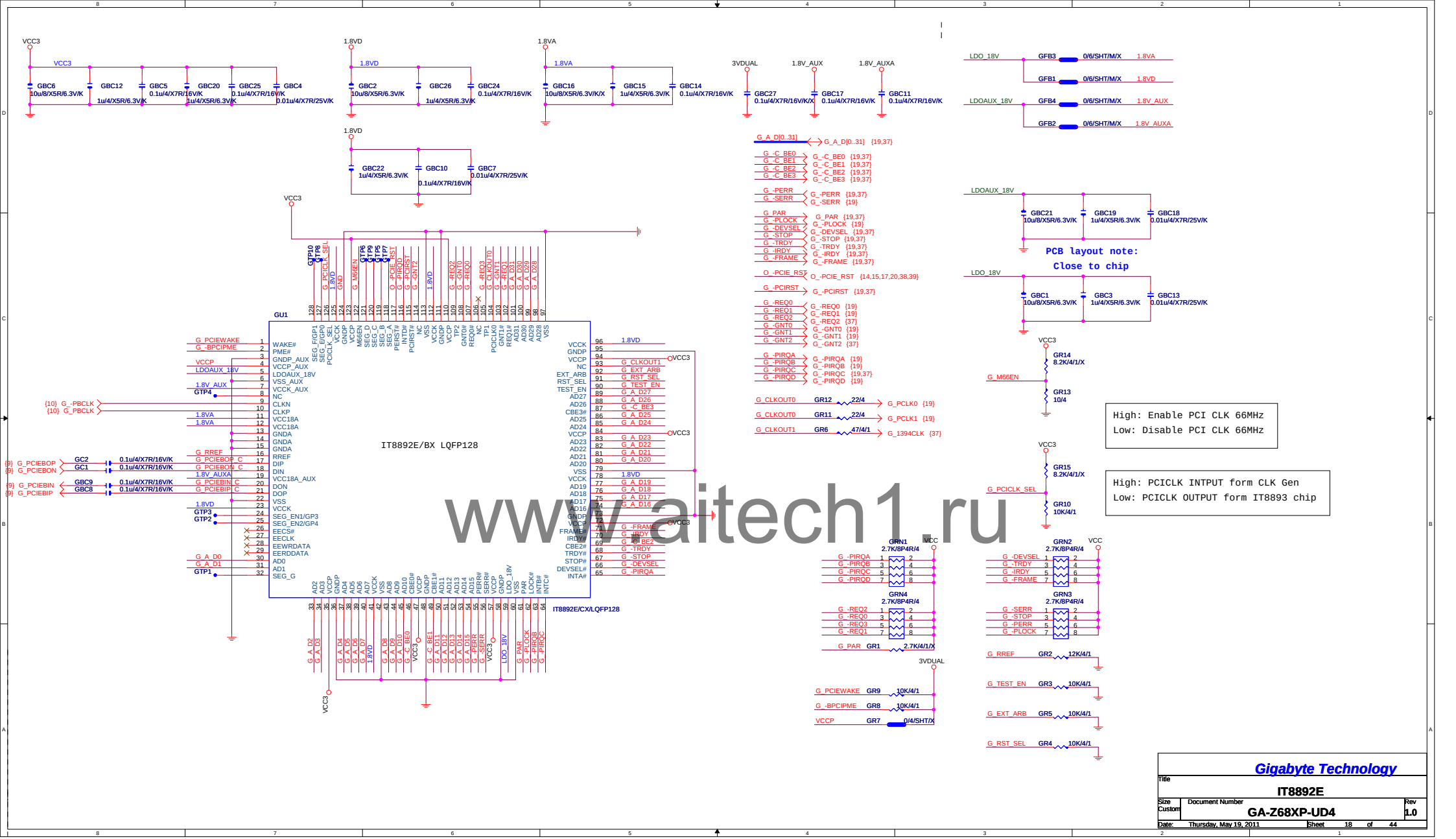
Gigabyte Technology		
Title: PCIE_X1 1,2		
Size: Custom	Document Number: GA-Z68XP-UD4	Rev: 1.0
Date: Thursday, May 19, 2011	Sheet 17 of 44	



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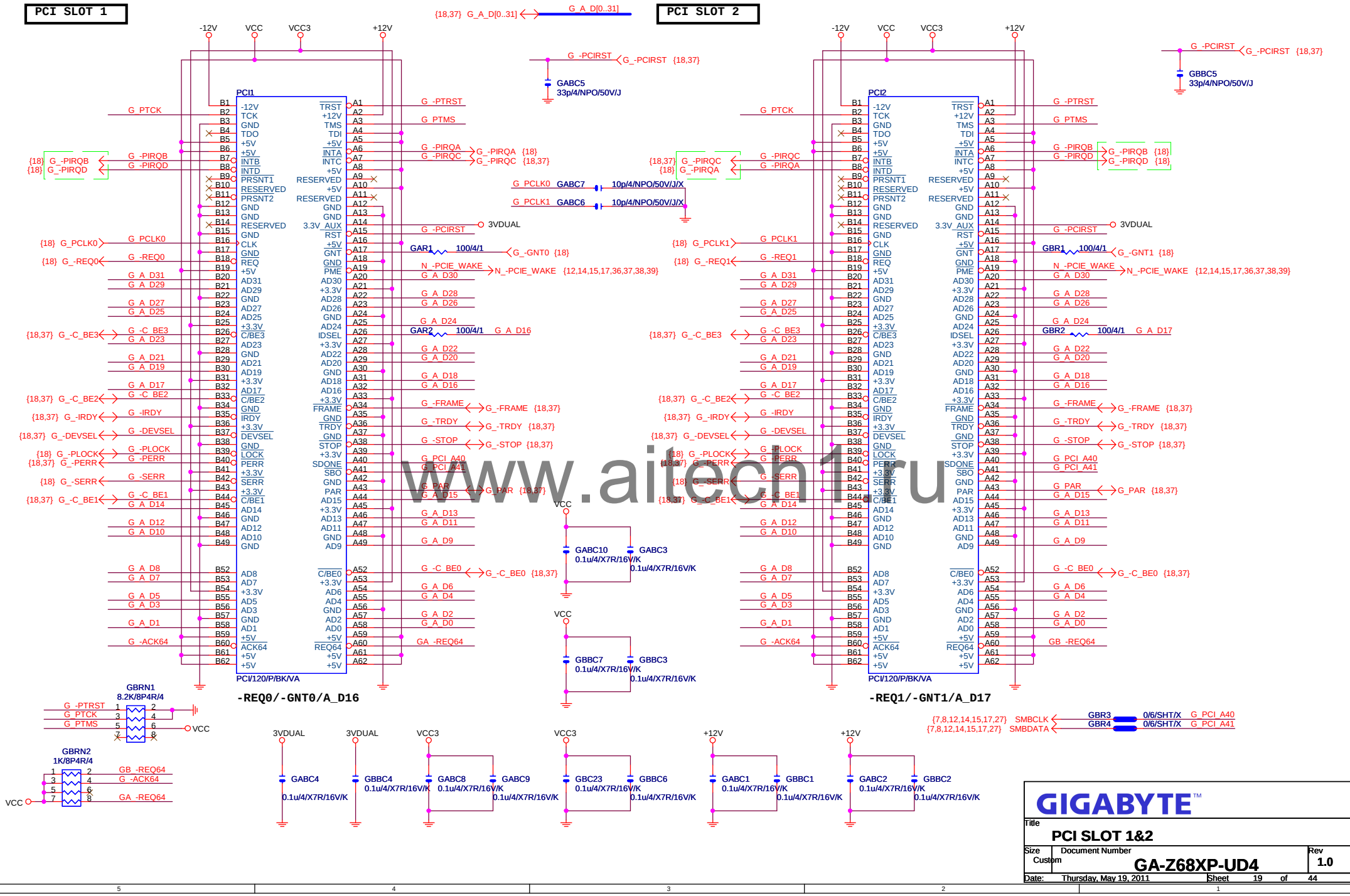

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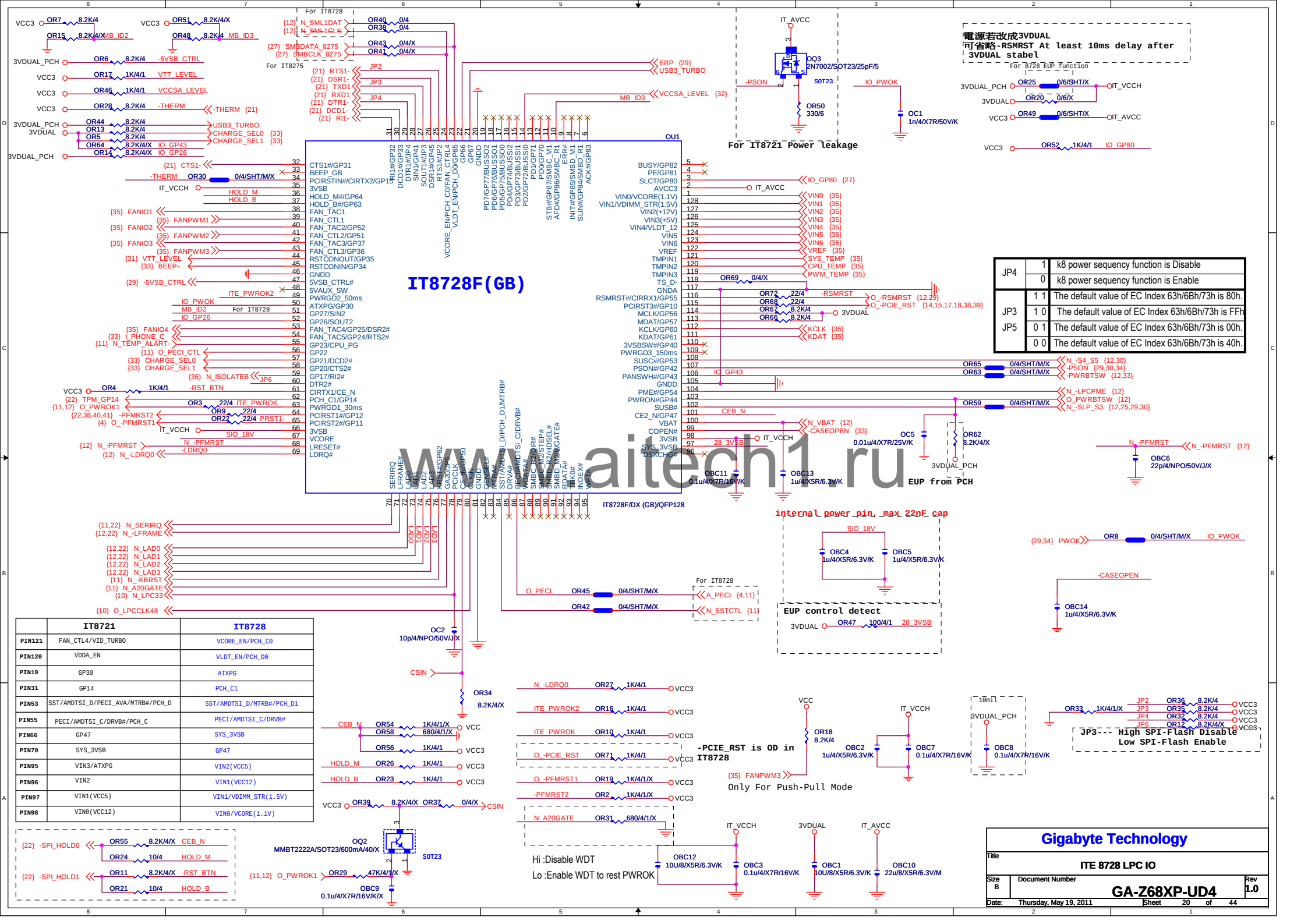

	IT8721	IT8728
PIN121	FAN_CTL4/VID_TURBO	VCORE_EN/PCH_C0
PIN120	VDDA_EN	VLDT_EN/PCH_D0
PIN19	GP30	ATXPG
PIN31	GP14	PCH_C1
PIN53	SST/AMDTSI_D/PECI_AVA/MTRB#/PCH_D	SST/AMDTSI_D/MTRB#/PCH_D1
PIN55	PECI/AMDTSI_C/DRVB#/PCH_C	PECI/AMDTSI_C/DRVB#
PIN66	GP47	SYS_3VSB
PIN70	SYS_3VSB	GP47
PIN95	VIN3/ATXPG	VIN2(VCC5)
PIN96	VIN2	VIN1(VCC12)
PIN97	VIN1(VCC5)	VIN1/VDIMM_STR(1.5V)
PIN98	VIN0(VCC12)	VIN0/VCORE(1.1V)

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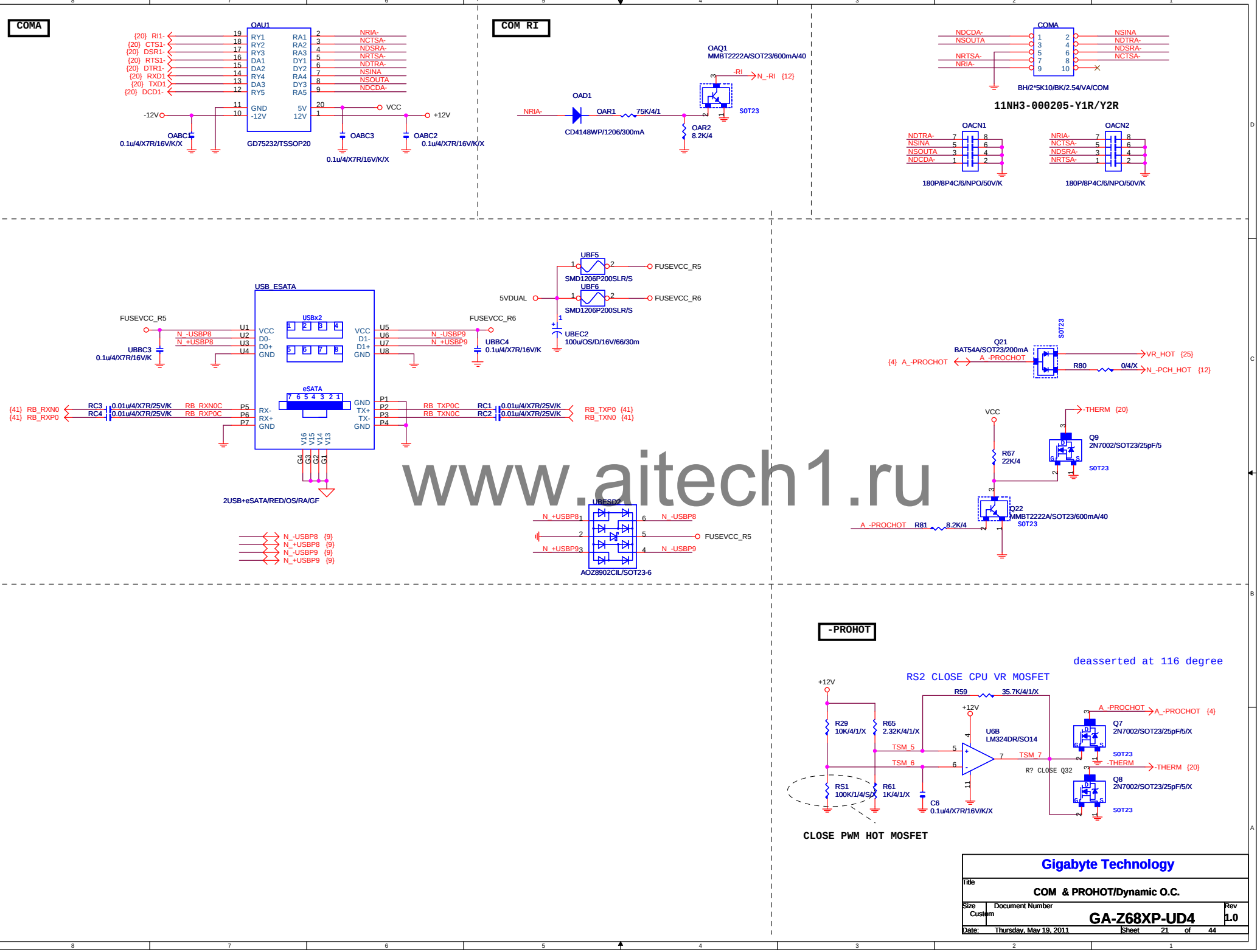

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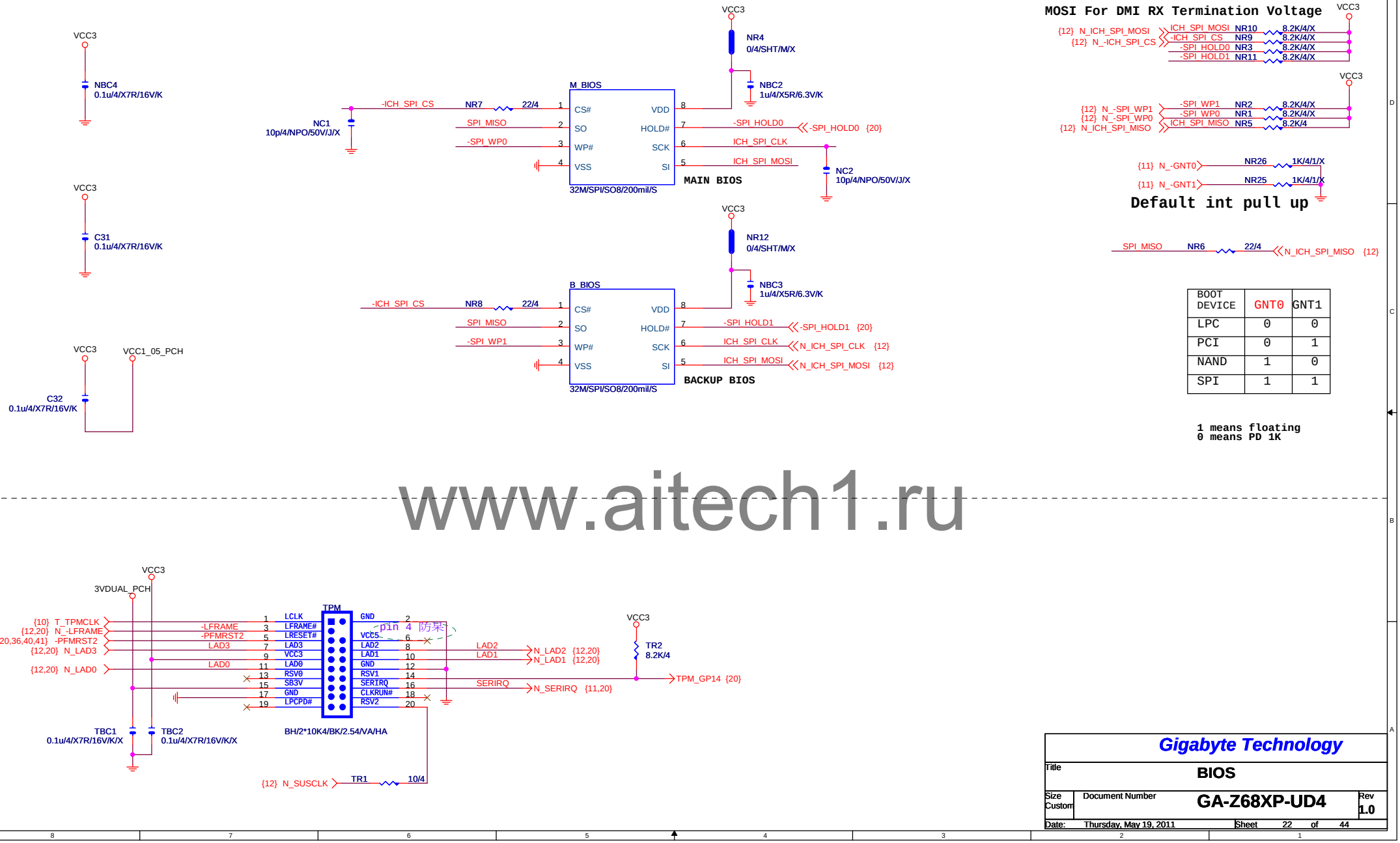

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Gigabyte Technology

Title: BIOS

Size: Custom | Document Number: GA-Z68XP-UD4 | Rev: 1.0

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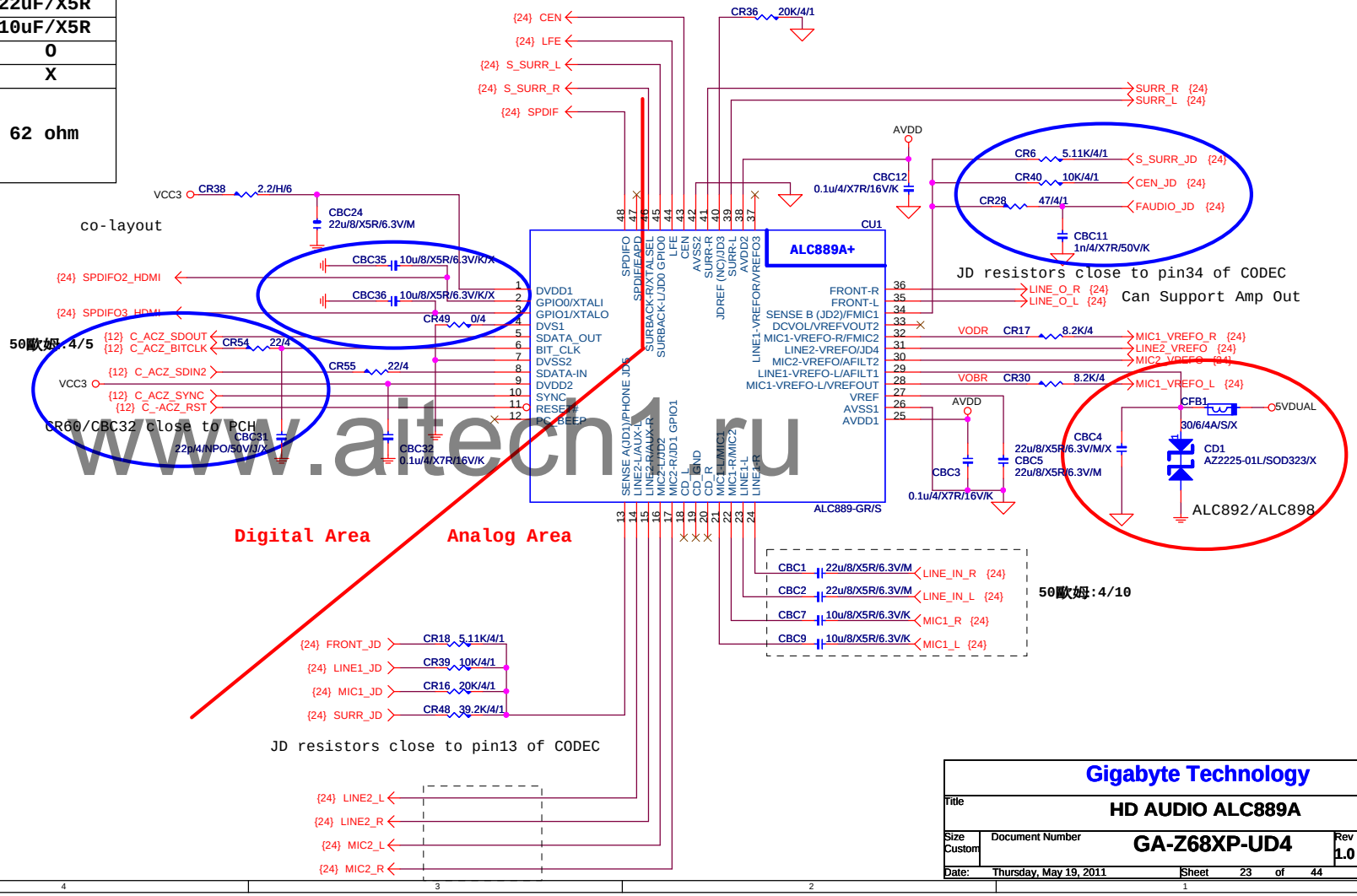
AZALIA CODEC **ALC889/ALC889B/ALC892/ALC898 Colay**

	ALC889	ALC889B	ALC898/ALC892
CR49	0	0	X
CBC36	X	X	10uF/X5R
CBC35	X	10uF/X5R	X
CR52	0	X	0
CR53	X	0	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R
CBC7/CBC9/CBC20/CBC15	10uF/X5R	10uF/X5R	10uF/X5R
CFB1/CD1/CBC4	X	X	0
CD2/CD3/CQ3/CQ4	0	0	X
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR21/CR47/ CR2/CR11/CR14/CR24	62 ohm	62 ohm	62 ohm



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Gigabyte Technology			
Title	HD AUDIO ALC889A		
Size: Custom	Document Number: GA-Z68XP-UD4		Rev: 1.0
Date: Thursday, May 19, 2011	Sheet 23 of 44		

CODEC POWER/EMI PAD

EUP

5VDUAL CQ4 CD4148WP/1206/300mA AVDD CQ3 78L05/SOT89/0.1A +12V CD3 CD4148WP/1206/300mA

CBC8 22u/8/X5R/6.3V/M CBC21 0.1u/4/X7R/16V/K/X

CD2 AZ2225-01L/SOD323

ADD CD2 For ESD PROTECT DIODE

CR44 0/6/X CR23 2.2/6 CR37 0/4/X

上ALC892時,此顆電容要保留

CR4 0/6/SHT/X

CESD1 AZ2025-04S/SOT23-5L/X

M2_L M2_R L2_R L2_L

{23} SPDIF SPDIF CBC14 0.01u/4/X7R/25V/K CR34 100/4/1 SPDIF_RCA CR33 200/4/1 CBC13 100p/4/NPO/50V/J

R_SPDIF

OPT RCA VCC G1 G2

FUSEVCC_R7

NEW "RCA_SPDIF-JST"

RCA/OPTI/SPDIFOUT/SHELL

{23} SPDIFO2_HDMI CR52 0/4 SPDIFO_HDMI

{23} SPDIFO3_HDMI CR53 0/4/X

CBC37 100p/4/NPO/50V/J

PIN SPDIF_O PH/1*2/BK/2.54/VA/D

For HDMI SPDIF

CESD5 AZ2025-04S/SOT23-5L/X

SPDIF SPDIFO_HDMI

AZALIA JACK

BTX AZALIA CONNECTOR

11NR6-403007-21R

CESD2 CESD4 CESD3 AZ2025-04S/SOT23-5L/X

AJ_A2 AJ_B2 AJ_C2 AJ_C5 AJ_B5 AJ_A5 BJ_B5 BJ_A5 BJ_C2 BJ_B2 BJ_C5 BJ_B2

AUDIOB

{23} LINE1_JD LINE1_JD AJ_A5 AJ_A2 GND LINE-IN

{23} FRONT_JD FRONT_JD AJ_B5 AJ_B2 GND LINE-OUT

{23} MIC1_JD MIC1_JD AJ_C5 AJ_C2 GND MIC-IN

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

BLUE LINE-IN

GREEN LINE-OUT

PINK MIC-IN

AUDIOA

{23} CEN_JD CEN_JD BJ_B5 BJ_B2 GND REAR

{23} SURR_JD SURR_JD BJ_C5 BJ_C2 GND CEN

{23} S_SURR_JD S_SURR_JD BJ_A5 BJ_A2 GND SIDE

2X3RP/26P/OR,BK,GY,BU,GE,PK/RA

Orange CEN/LFE

Black SURROUND

Gray SURROUND SIDE

LINE-OUT

{23} LINE_O_R CEC2 100u/OS/D/16V/66/30m CR7 62/4

{23} LINE_O_L CEC3 100u/OS/D/16V/66/30m CR9 62/4

CR10 22K/4 CR8 22K/4 AJ_B5 AJ_B2

CBC23 180p/4/NPO/50V/J CBC26 180p/4/NPO/50V/J

LINE-IN

{23} LINE_IN_R CR5 62/4 AJ_A5

{23} LINE_IN_L CR13 62/4 AJ_A2

CBC18 180p/4/NPO/50V/J CBC27 180p/4/NPO/50V/J

MIC-IN

{23} MIC1_R CR29 62/4 AJ_C5

{23} MIC1_L CR32 62/4 AJ_C2

{23} MIC1_VREFO_L

{23} MIC1_VREFO_R

CBC19 180p/4/NPO/50V/J CBC22 180p/4/NPO/50V/J

SURROUND

EMI

{23} SURR_R CEC5 100u/OS/D/16V/66/30m CR46 62/4

{23} SURR_L CEC7 100u/OS/D/16V/66/30m CR19 62/4

CR20 22K/4 CR45 22K/4 BJ_C5 BJ_C2

CBC29 180p/4/NPO/50V/J CBC28 180p/4/NPO/50V/J

CEN/LFE

EMI

{23} LFE CEC9 100u/OS/D/16V/66/30m CR50 62/4

{23} CEN CEC10 100u/OS/D/16V/66/30m CR41 62/4

CR42 22K/4 CR51 22K/4 BJ_B5 BJ_B2

CBC25 180p/4/NPO/50V/J CBC34 180p/4/NPO/50V/J

SURR BACK

EMI

{23} S_SURR_R CEC8 100u/OS/D/16V/66/30m CR21 62/4

{23} S_SURR_L CEC4 100u/OS/D/16V/66/30m CR47 62/4

CR43 22K/4 CR22 22K/4 BJ_A5 BJ_A2

CBC33 180p/4/NPO/50V/J CBC30 180p/4/NPO/50V/J

AZALIA FRONT PANEL

CQ2 BAT54A/SOT23/200mA CQ1 BAT54A/SOT23/200mA SOT23

{23} LINE2_VREFO CR25 8.2K/4 CR15 8.2K/4

{23} MIC2_VREFO CR12 8.2K/4 CR3 8.2K/4

EMI

{23} MIC2_L {23} MIC2_R CBC20 10u/8/X5R/6.3V/K CBC15 10u/8/X5R/6.3V/K CR2 62/4 CR11 62/4 M2_L M2_R

{23} FAUDIO_JD L2_R L2_L CR14 62/4 CR24 62/4

CR1 0/4/X

F_AUDIO bh/2*5k8/bk/2.54/va/[11nh3-000205-p1r]

CR27 22K/4 CR26 22K/4 CR56 8.2K/4/X CR35 20K/4/1 CR31 39.2K/4/1

C_-ACZ_DET {12}

Digital Area 3VDUAL

CBC10 180p/4/NPO/50V/J CBC16 180p/4/NPO/50V/J CBC17 180p/4/NPO/50V/J CBC6 180p/4/NPO/50V/J

{23} LINE2_R {23} LINE2_L CEC6 CEC1 100u/OS/D/16V/66/30m L2_R L2_L

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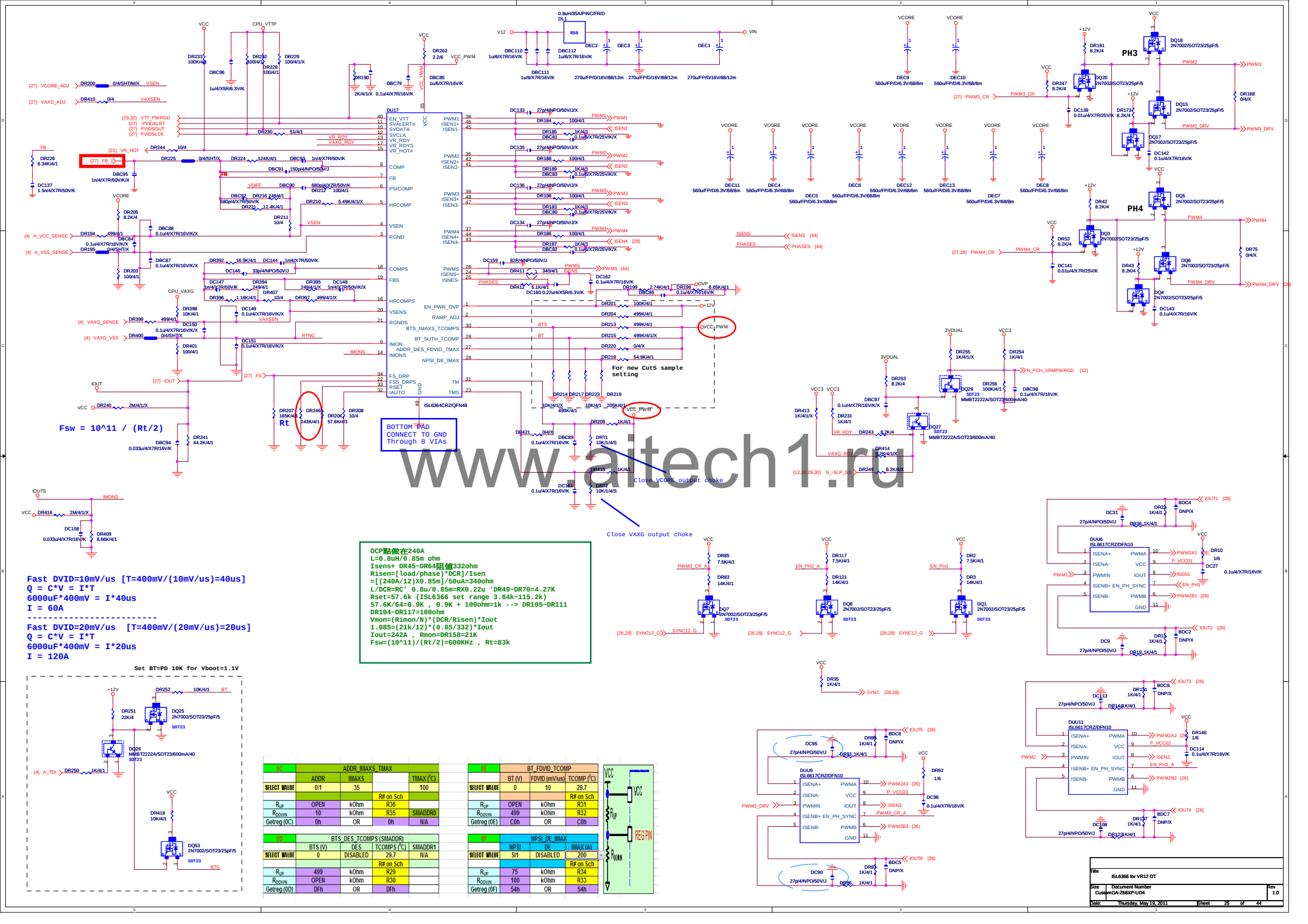
Gigabyte Technology

Title: AUDIO JACK

Size: Custom Document Number: GA-Z68XP-UD4 Rev: 1.0

Date: Thursday, May 19, 2011 Sheet 24 of 44



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DC	ADDR_IMAXS_TMAX			
	ADDR	IMAXS		TMAX (°C)
SELECT VALUE	0/1	35		100
			R# on Sch	
R_{UP}	OPEN	kOhm	R36	
R_{DOWN}	10	kOhm	R35	SMADDR0
Getreg (0C)	0h	OR	0h	N/A

DE	BT_FDVID_TCOMP		
	BT (V)	FDVID (mV/us)	TCOMP (°C)
SELECT VALUE	0	10	29.7
			R# on Sch
R_{UP}	OPEN	kOhm	R31
R_{DOWN}	499	kOhm	R32
Getreg (0E)	C0h	OR	C0h

DD	BTS_DES_TCOMPS (SMADDR)			
	BTS (V)	DES	TCOMPS (°C)	SMADDR1
SELECT VALUE	0	DISABLED	29.7	N/A
			R# on Sch	
R_{UP}	499	kOhm	R29	
R_{DOWN}	OPEN	kOhm	R30	
Getreg (0D)	DFh	OR	DFh	

DF	NPSI_DE_IMAX		
	NPSI	DE	IMAX (A)
SELECT VALUE	S1	DISABLED	200
			R# on Sch
R_{UP}	75	kOhm	R34
R_{DOWN}	100	kOhm	R33
Getreg (0F)	54h	OR	54h

Title	ISL6366 for VR12 DT
Size	Document Number: CustomGA-Z68XP-UD4
Rev	1.0
Date:	Thursday, May 19, 2011
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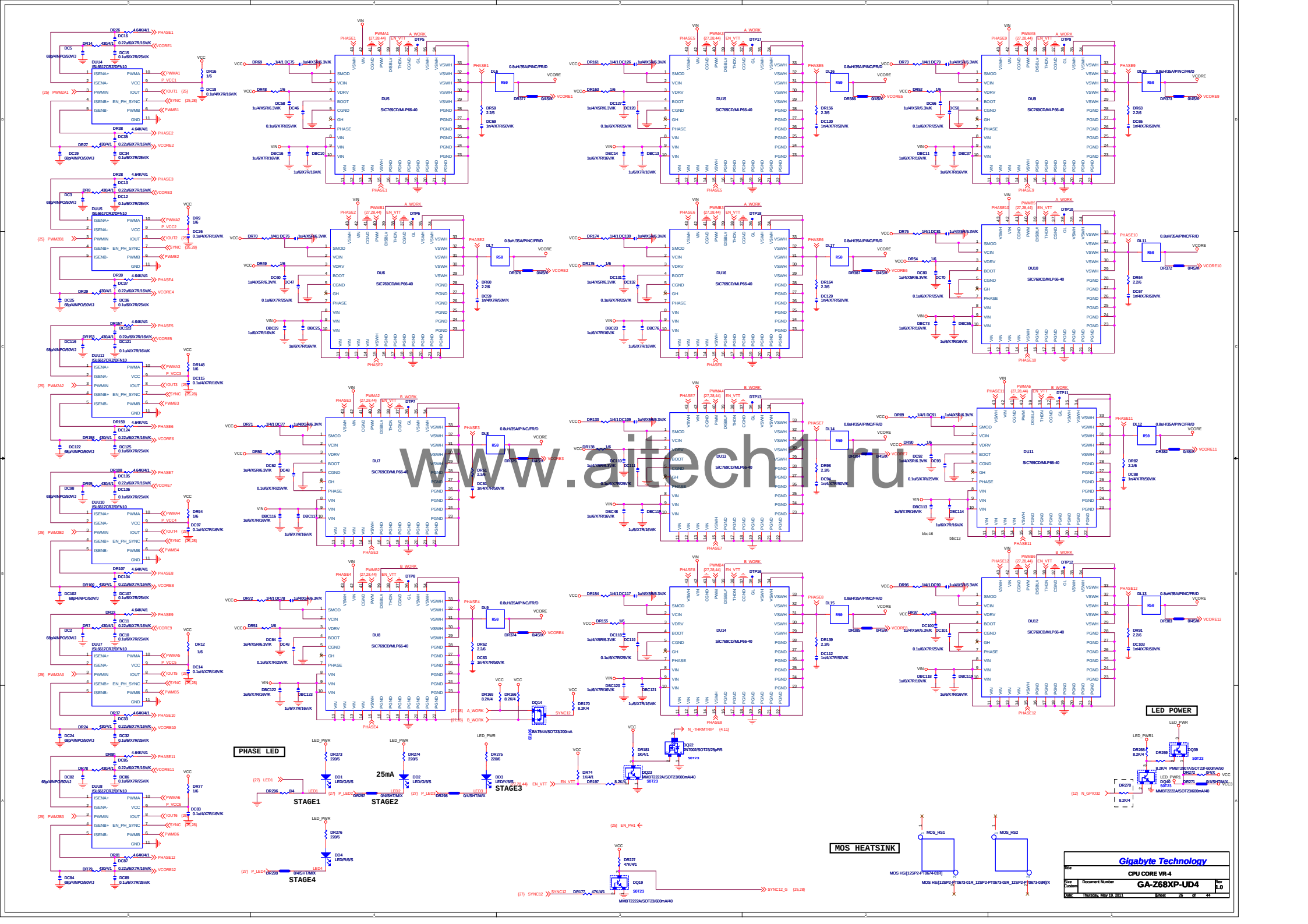

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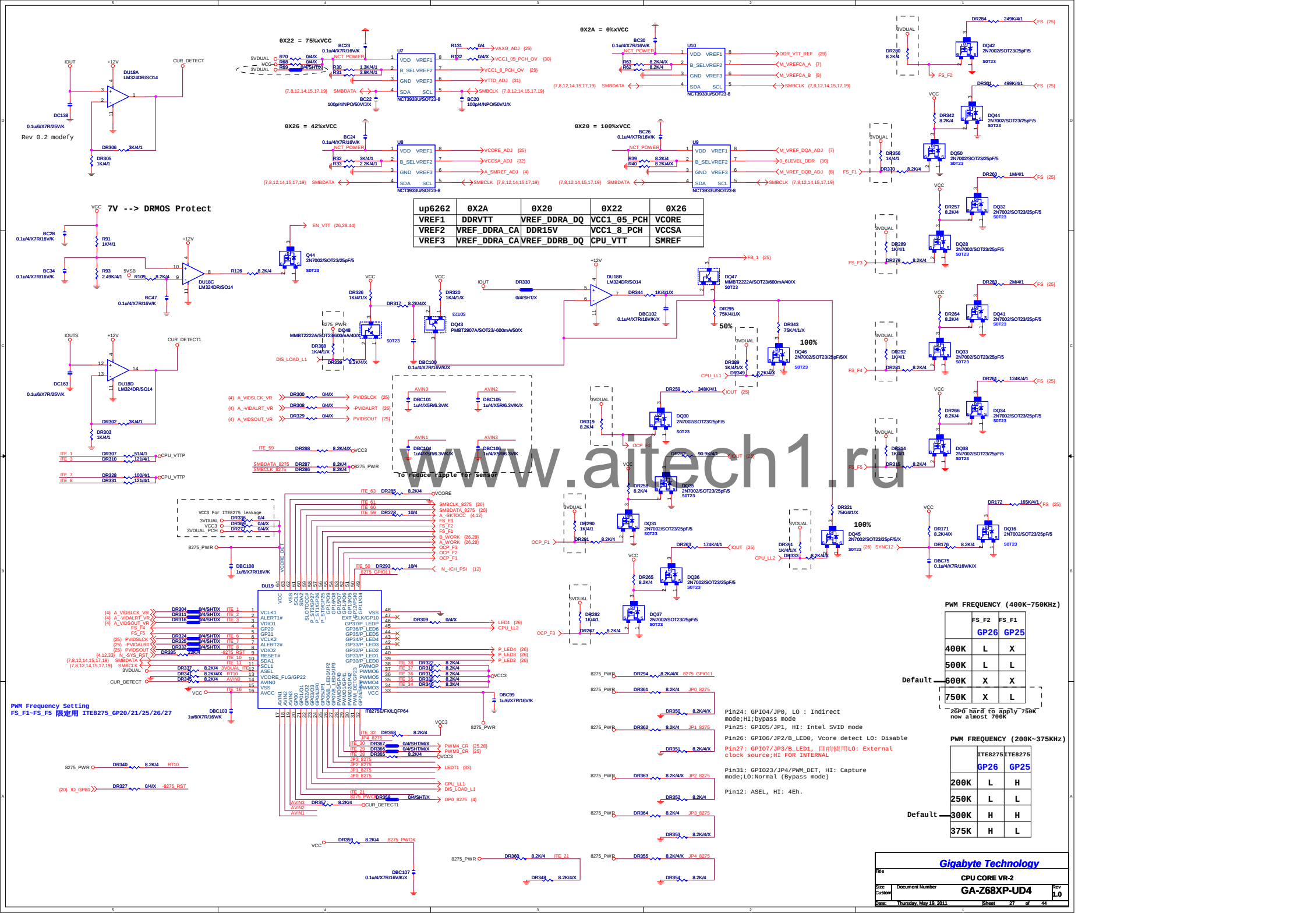

up6262	0X2A	0X20	0X22	0X26
VREF1	DDRVTT	VREF_DDRA_DQ	VCC1_05_PCH	VCORE
VREF2	VREF_DDRA_CA	DDR15V	VCC1_8_PCH	VCCSA
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	CPU_VTT	SMREF

PWM Frequency Setting
FS_F1~FS_F5 限定用 ITE8275_GP20/21/25/26/27

PWM FREQUENCY (400K~750KHz)

	FS_F2	FS_F1
	GP26	GP25
400K	L	X
500K	L	L
Default 600K	X	X
750K	X	L

2GP0 hard to apply 750K now almost 700K

PWM FREQUENCY (200K~375KHz)

	ITE8275	ITE8275
	GP26	GP25
200K	L	H
250K	L	L
Default 300K	H	H
375K	H	L

Gigabyte Technology			
Title	CPU CORE VR-2		
Size: Custom	Document Number: GA-Z68XP-UD4		Rev: 1.0
Date: Thursday, May 19, 2011	Sheet 27 of 44		

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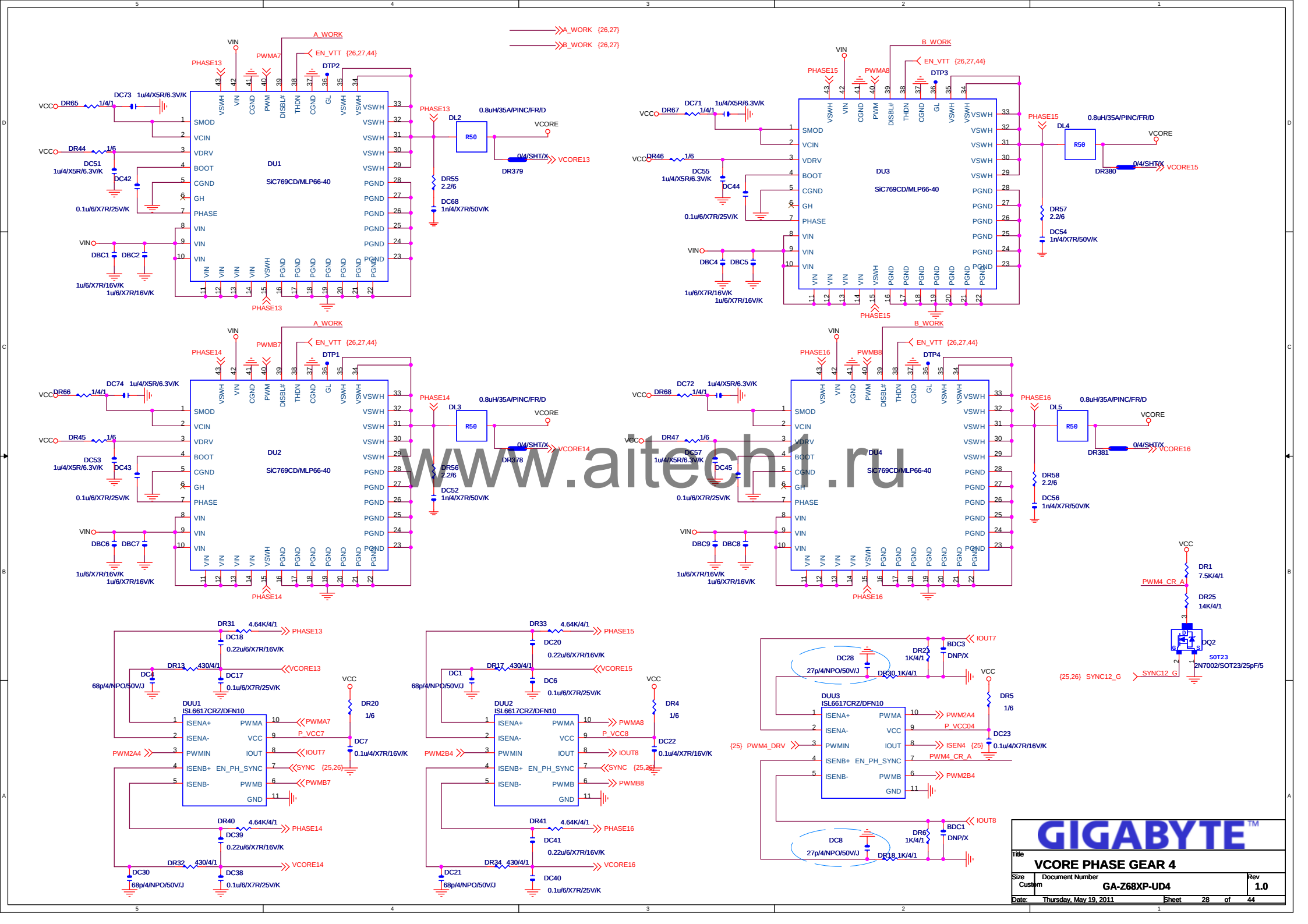

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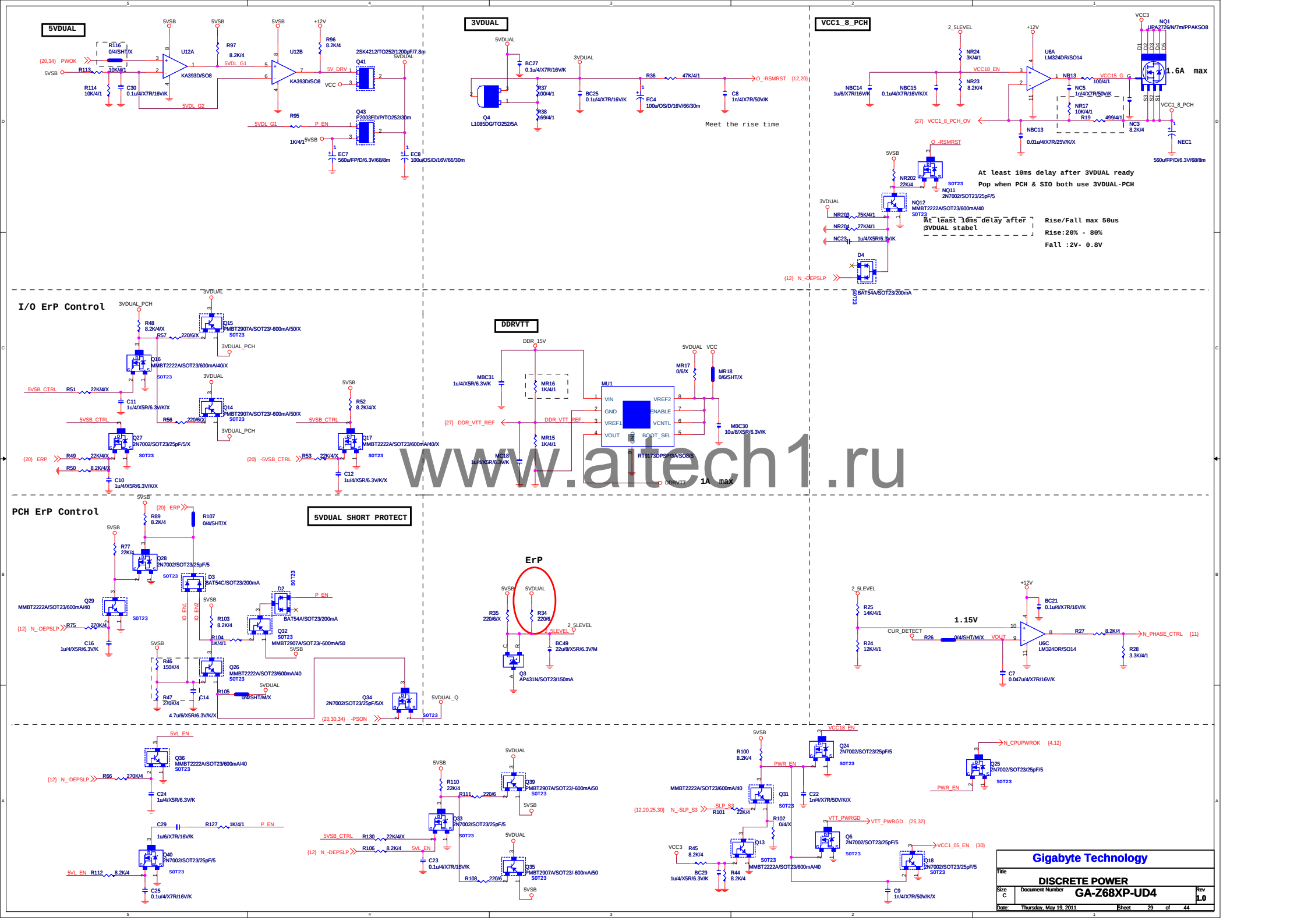

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Gigabyte Technology			
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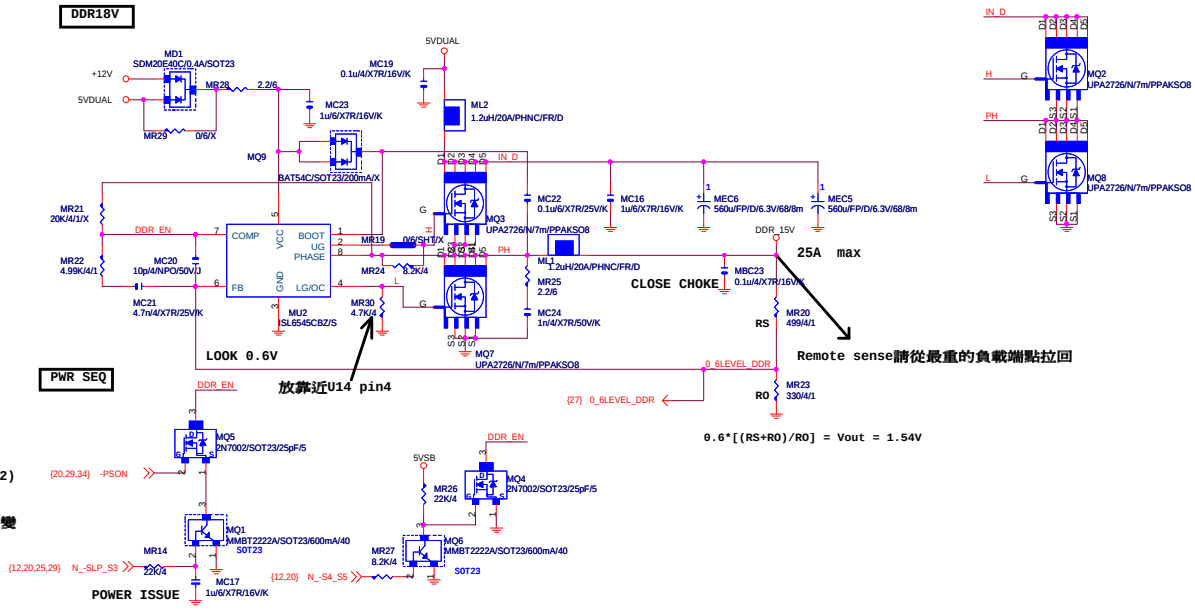
Size: C	Document Number: GA-Z68XP-UD4		Rev: 1.0
Date: Thursday, May 19, 2011	Sheet 29 of 44		



OCP : Ipeak=(2xIocsetxRocset)/Rdson
Iocset=21.5uA , Rocset=4.7k

OCP : Ipeak=(2xIocsetxRocset)/Rdson
=(2x21.5ux4.7k)/(7m/2)
=57.74A

注意 : Rocset的阻值要依據Lo side Rdson改變
一般Ipeak設定在50~60A即可

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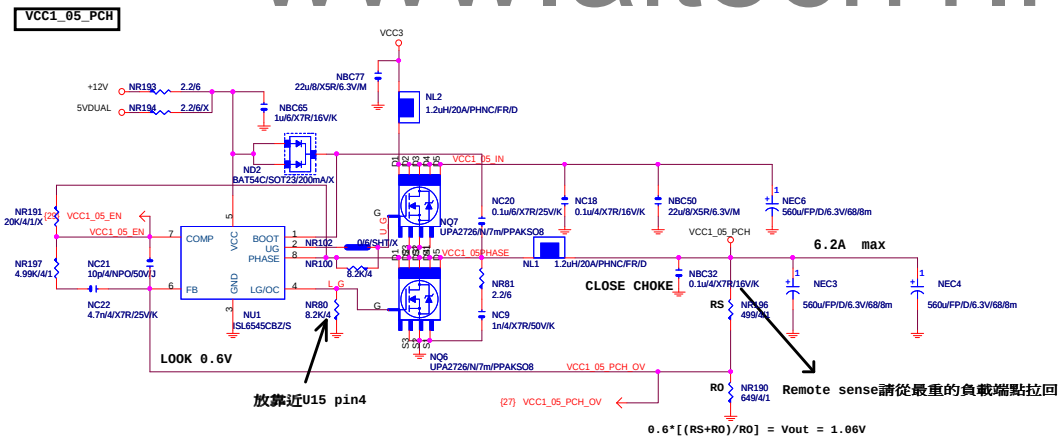
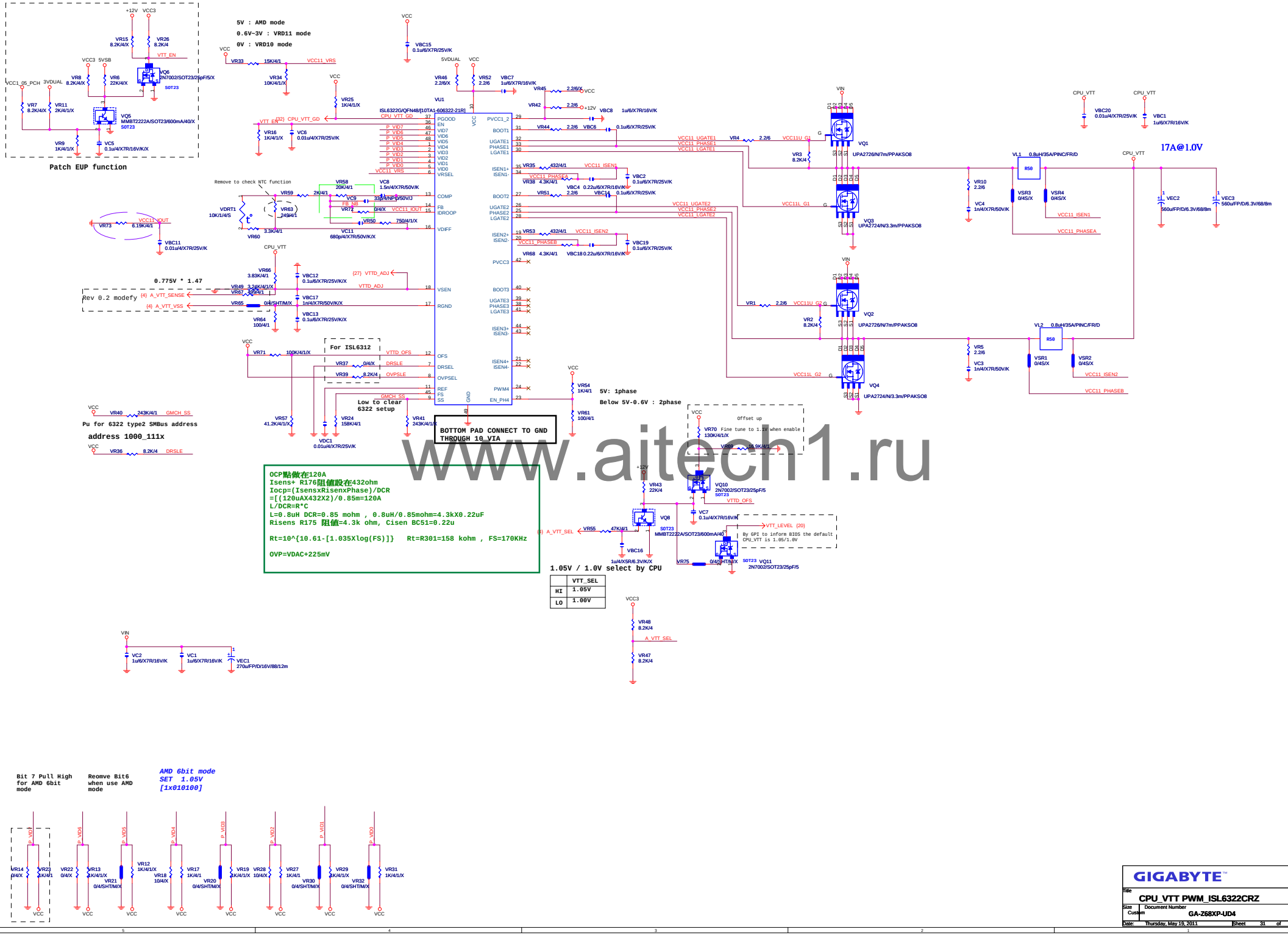


OCP : Ipeak=(2xIocsetxRocset)/Rdson
Iocset=21.5uA , Rocset=8.2k

OCP : Ipeak=(2xIocsetxRocset)/Rdson
=(2x21.5ux8.2k)/7m
=50.37A

注意 : Rocset的阻值要依據Lo side Rdson改變
一般Ipeak設定在50~60A即可

Gigabyte Technology		
Title: DDR_15V		
Size: C	Document Number: GA-Z68XP-UD4	Rev: 1.0
Date: Thursday, May 19, 2011	Sheet 30 of 44	



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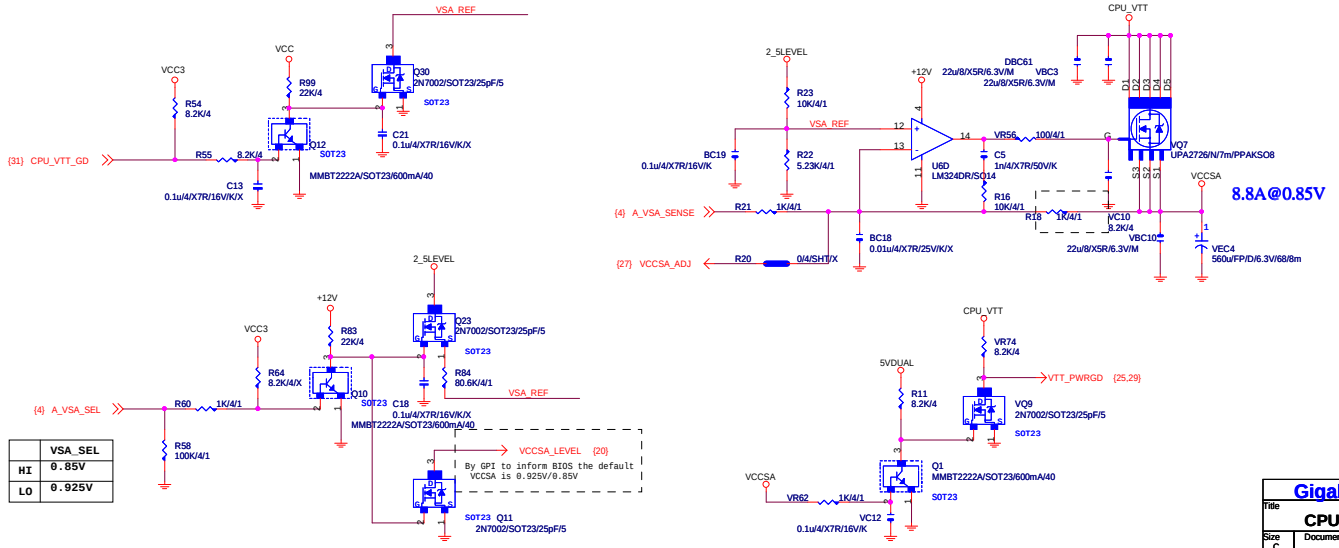
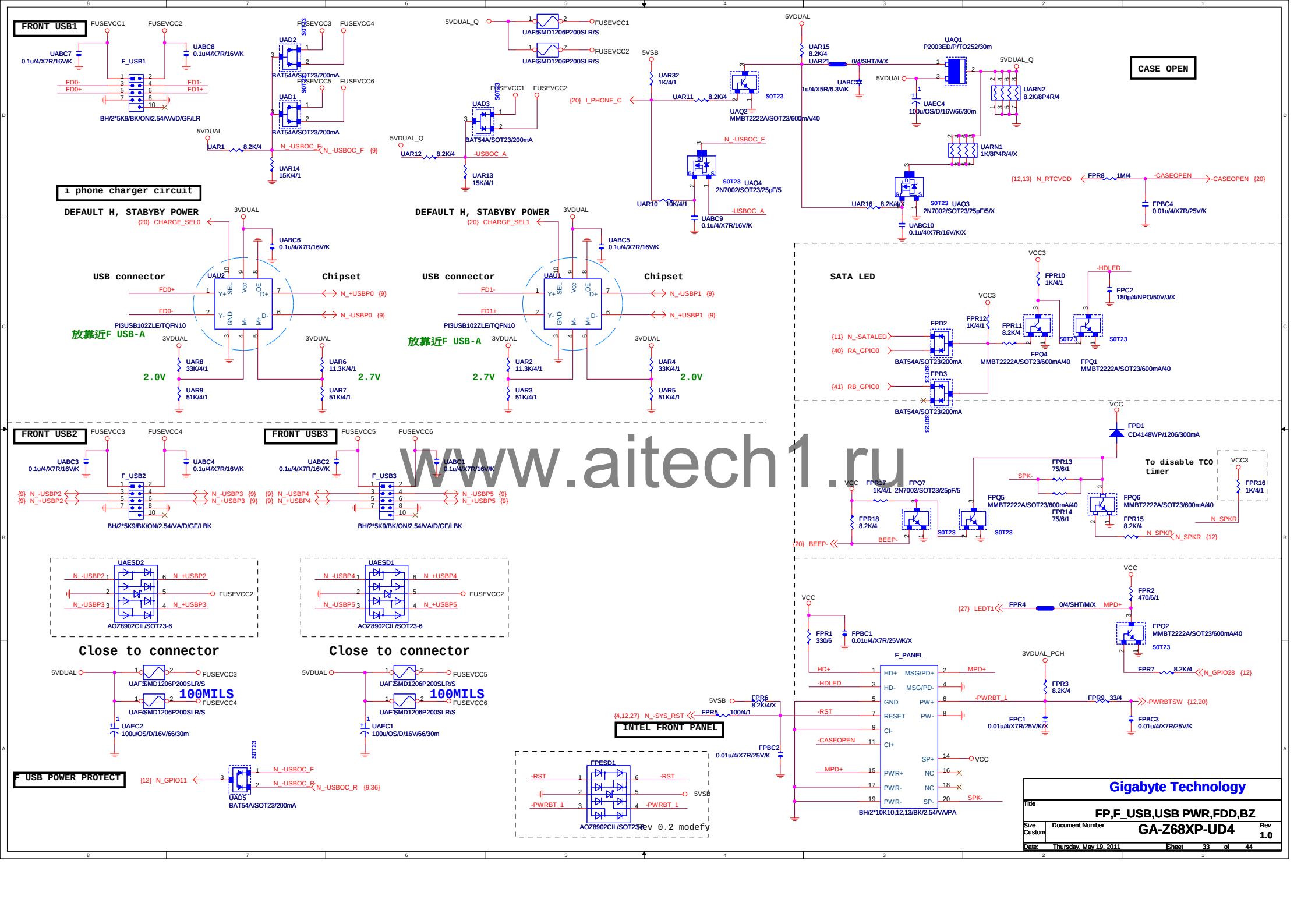
VCC_SA



Title	CPU VTT PWM_ISL6312
Size	C
Document Number	GA-Z68XP-UD4
Rev	1.0
Date:	Thursday, May 19, 2011
Sheet	32 of 44

Gigabyte Technology



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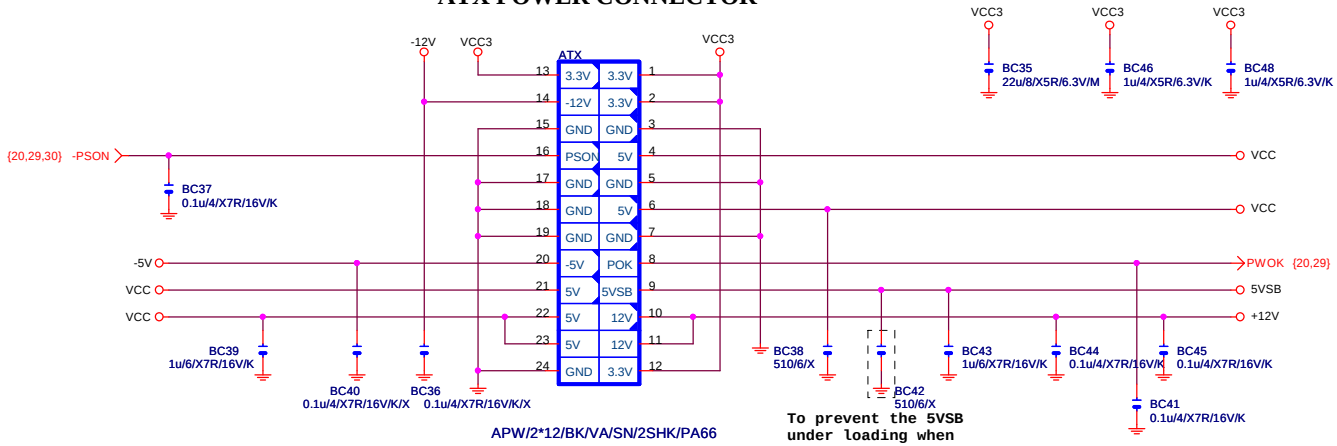
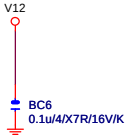
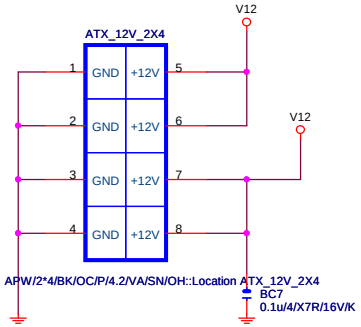
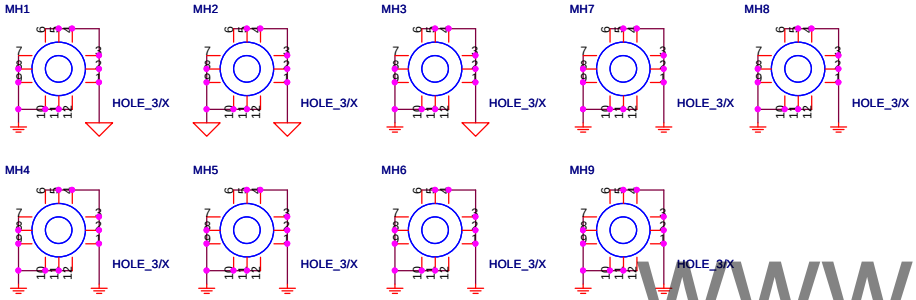
ATX POWER CONNECTOR

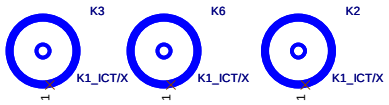


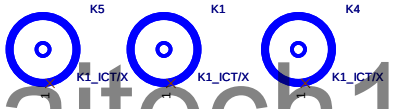
To prevent the 5VSB under loading when boot

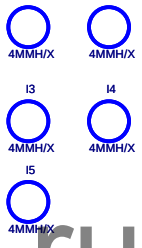


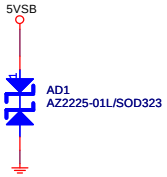












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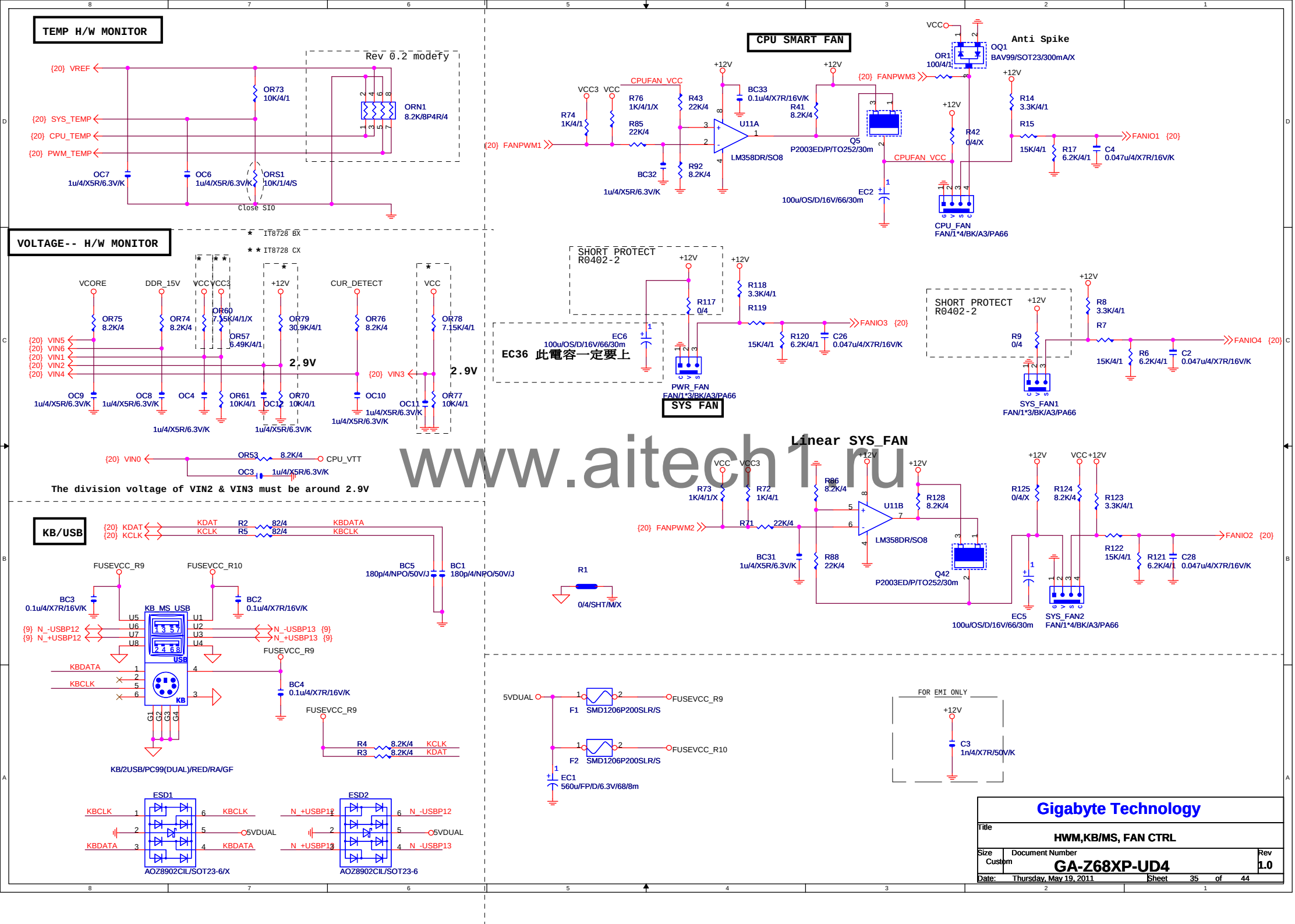
Gigabyte Technology		
Title: ATX POWER CONNECTOR		
Size: Custom	Document Number: GA-Z68XP-UD4	Rev: 1.0
Date: Thursday, May 19, 2011	Sheet 34 of 44	



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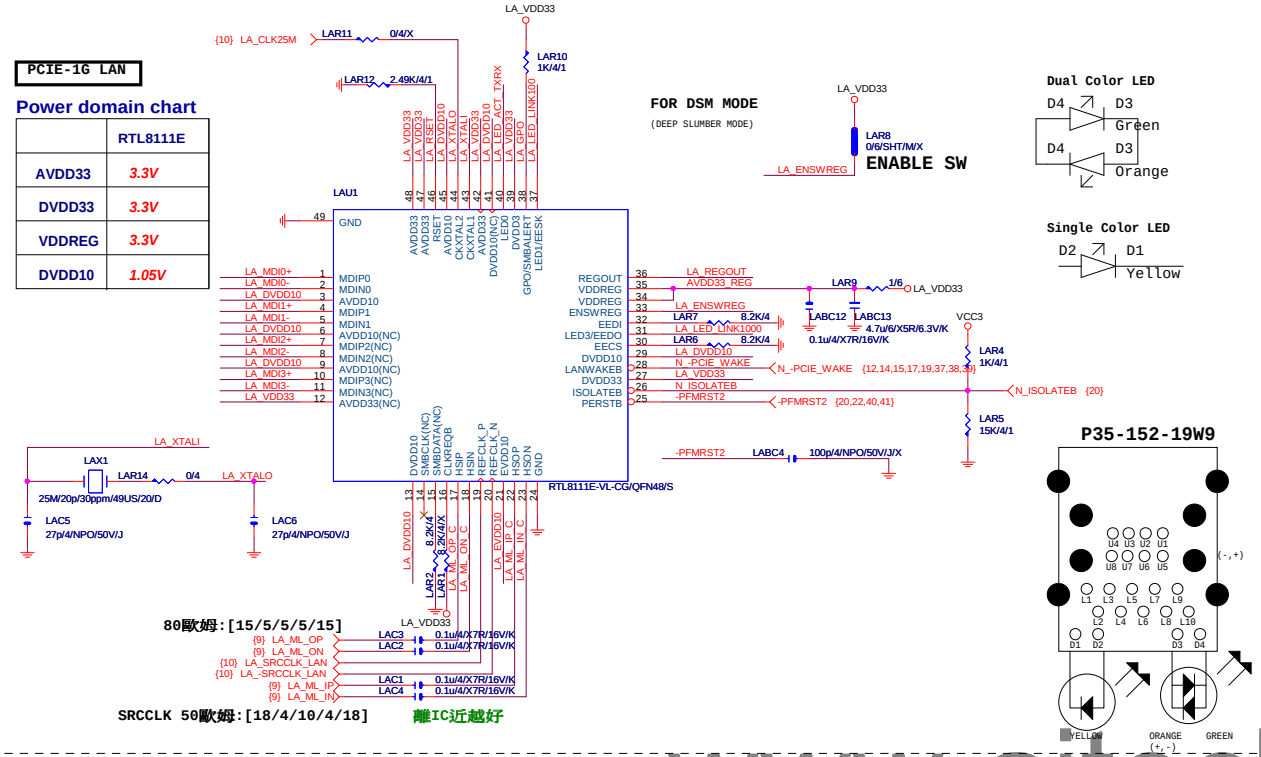
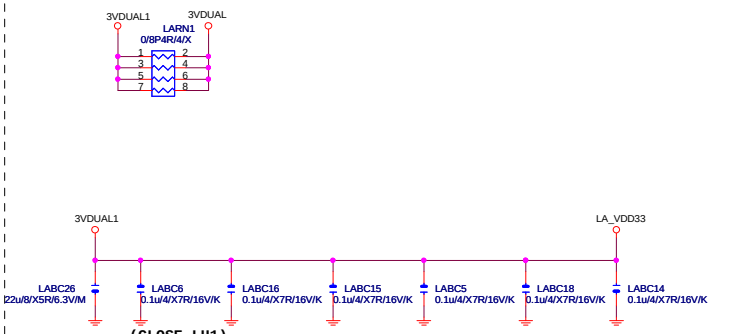
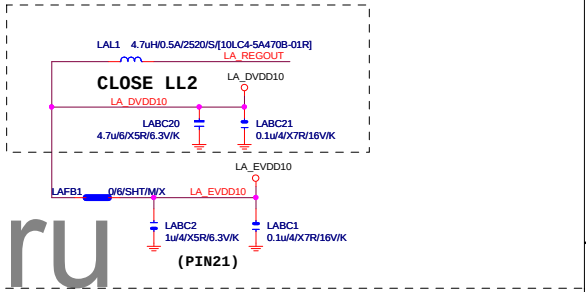
PCIE-1G LAN

Power domain chart

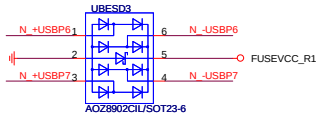
	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V

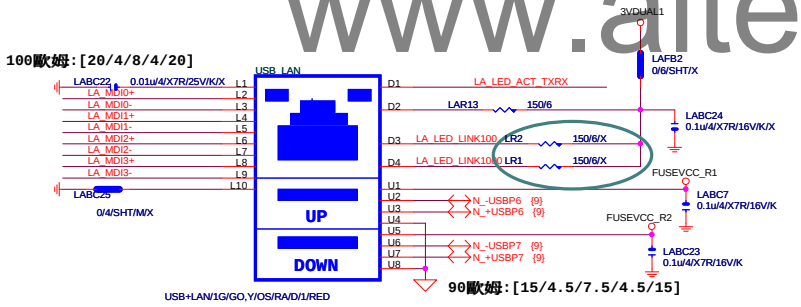


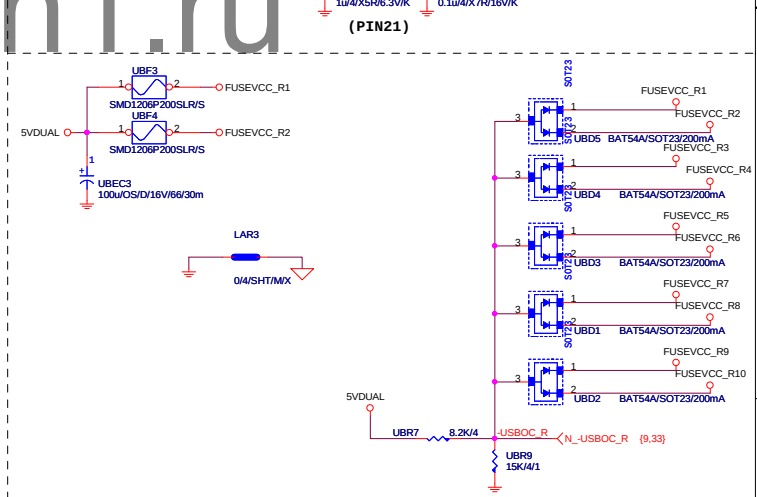




USB30_LAN CONNECTOR







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Gigabyte Technology			
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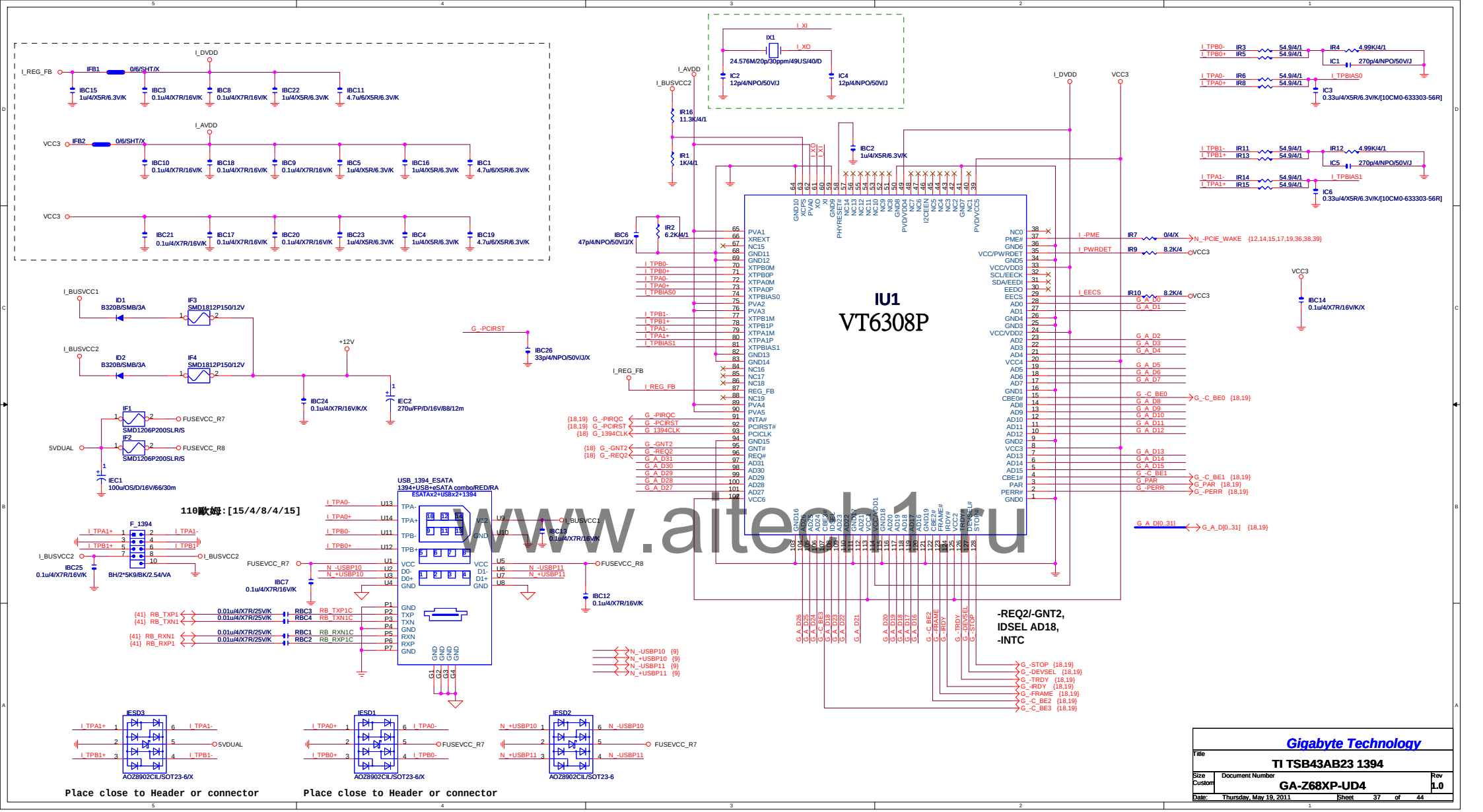
Size: Custom	Document Number: GA-Z68XP-UD4		Rev: 1.0
Date: Thursday, May 19, 2011	Sheet 36 of 44		



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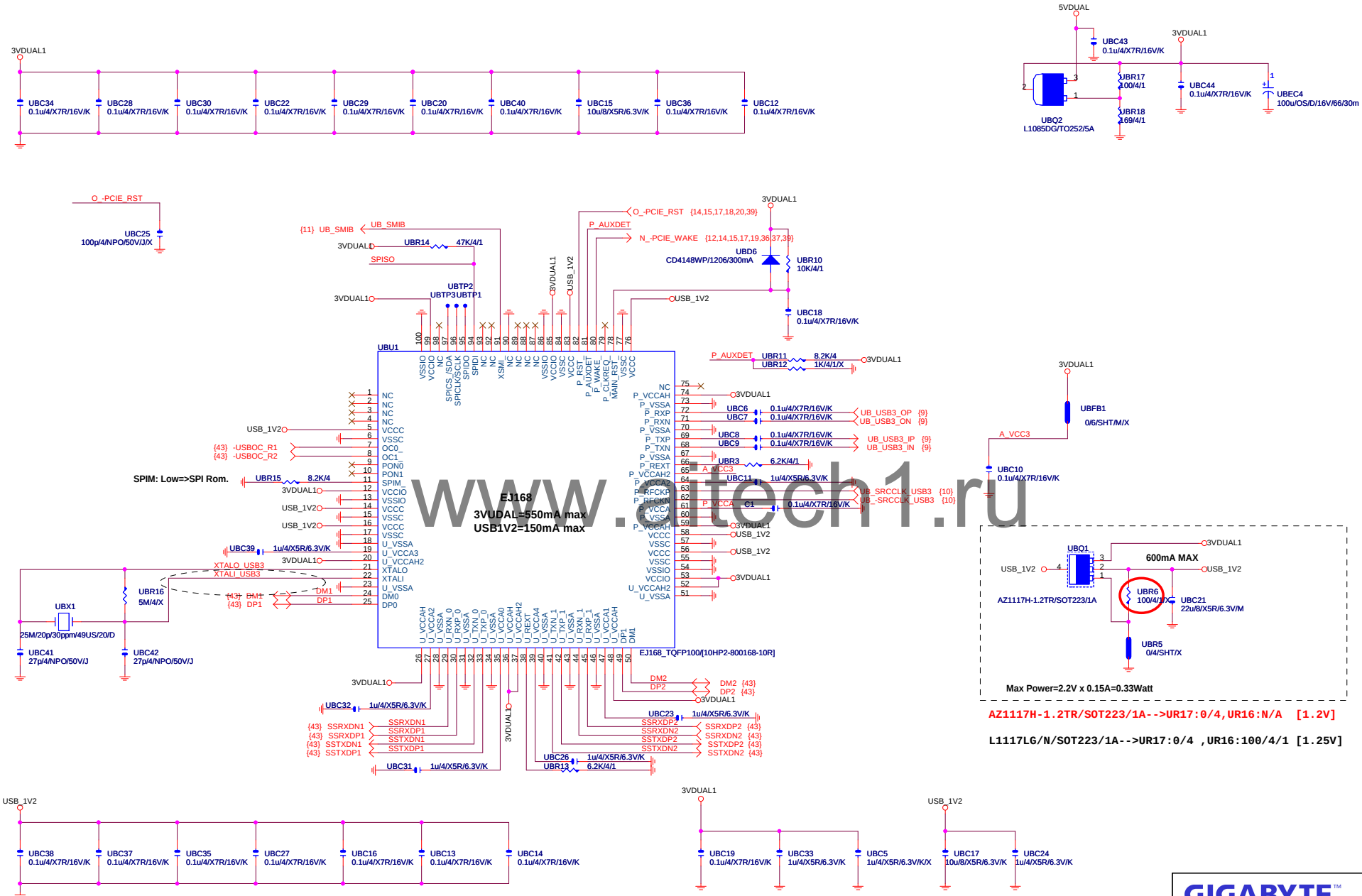

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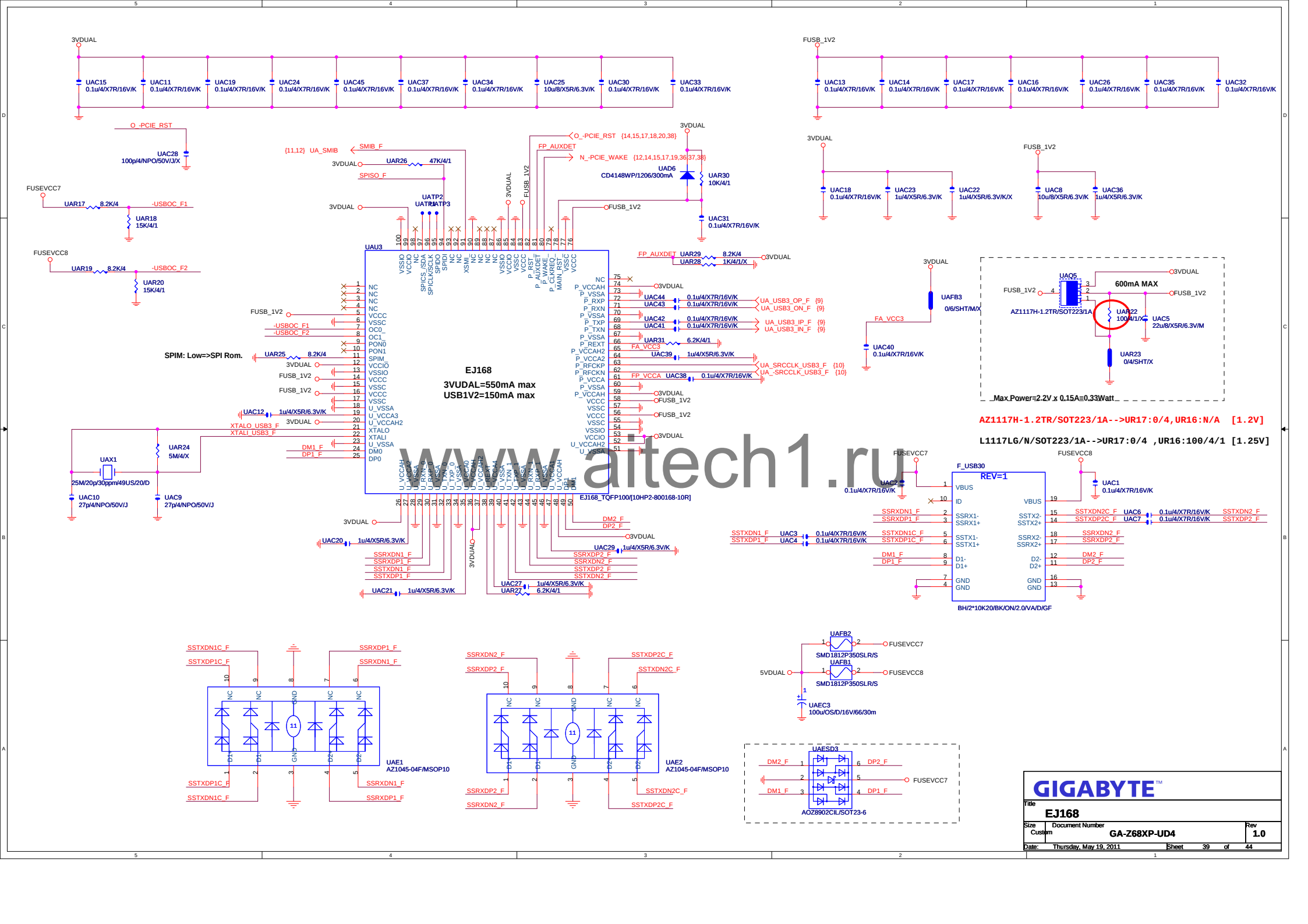

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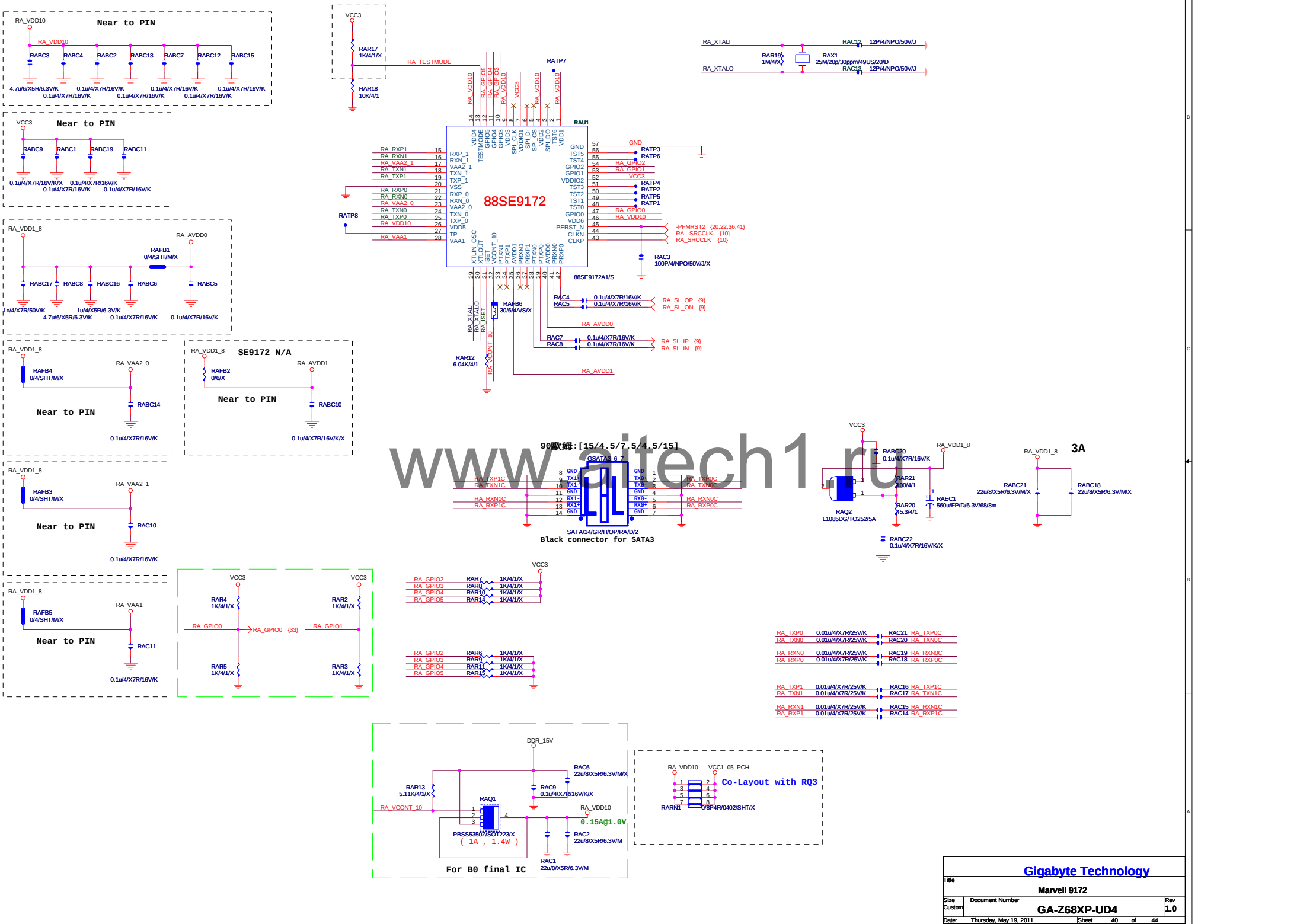

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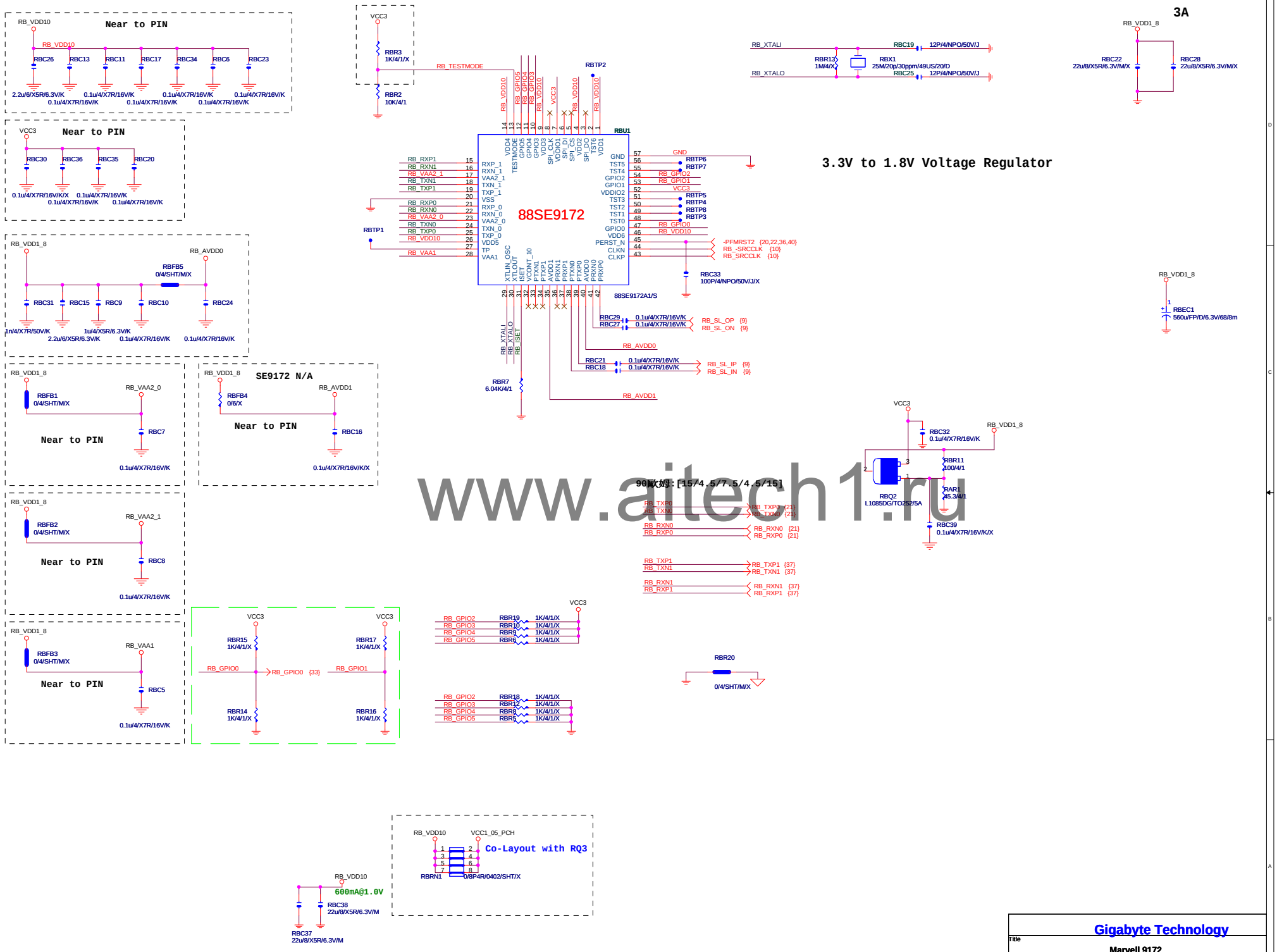

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Title	Gigabyte Technology
	Marvell 9172
Size / Custom	Document Number: GA-Z68XP-UD4
Rev	1.0
Date:	Thursday, May 19, 2011
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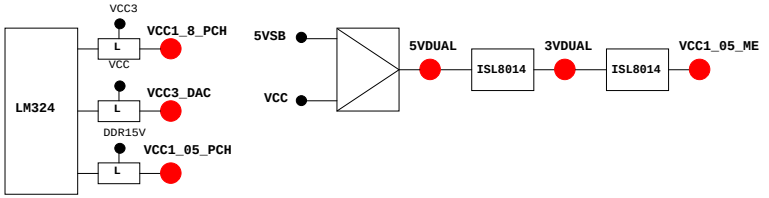
PCH GPIO LIST TABLE

PIN NAME	PWR	AFTER/PLTRST	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI	-PECI_REQ	N/A
GP1/TACH1	MAIN		GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN		GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO	GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY		NATIVE	OC5#	N/A
GP10/OC6#	STBY		NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI	GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	OC7#	N/A
GP15	STBY	L	GPO	GPIO15	N/A
GP16	MAIN		GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	ICH_FAN_TACH0	N/A
GP18	MAIN		NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN		GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN		NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN		GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN		NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO	TLS	P/U 8.2K 3VDUAL
GP25	STBY		NATIVE	-CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY		NATIVE	-ACZ_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI	N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO	MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO	LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	GPIO35	P/U 8.2K VCC3
GP36	MAIN		GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN		GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI	VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	-LAN_DSM	P/U 8.2K VCC3
GP40	STBY		NATIVE	OC1#	N/A
GP41	STBY		NATIVE	OC2#	N/A
GP42	STBY		NATIVE	OC3#	N/A
GP43	STBY		NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE	N/A	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY		NATIVE	PSI LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN	EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN	VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY		NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

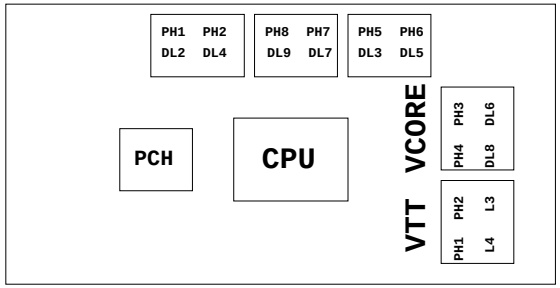
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMBC_R	空 PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSSO0	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

8IBP:
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

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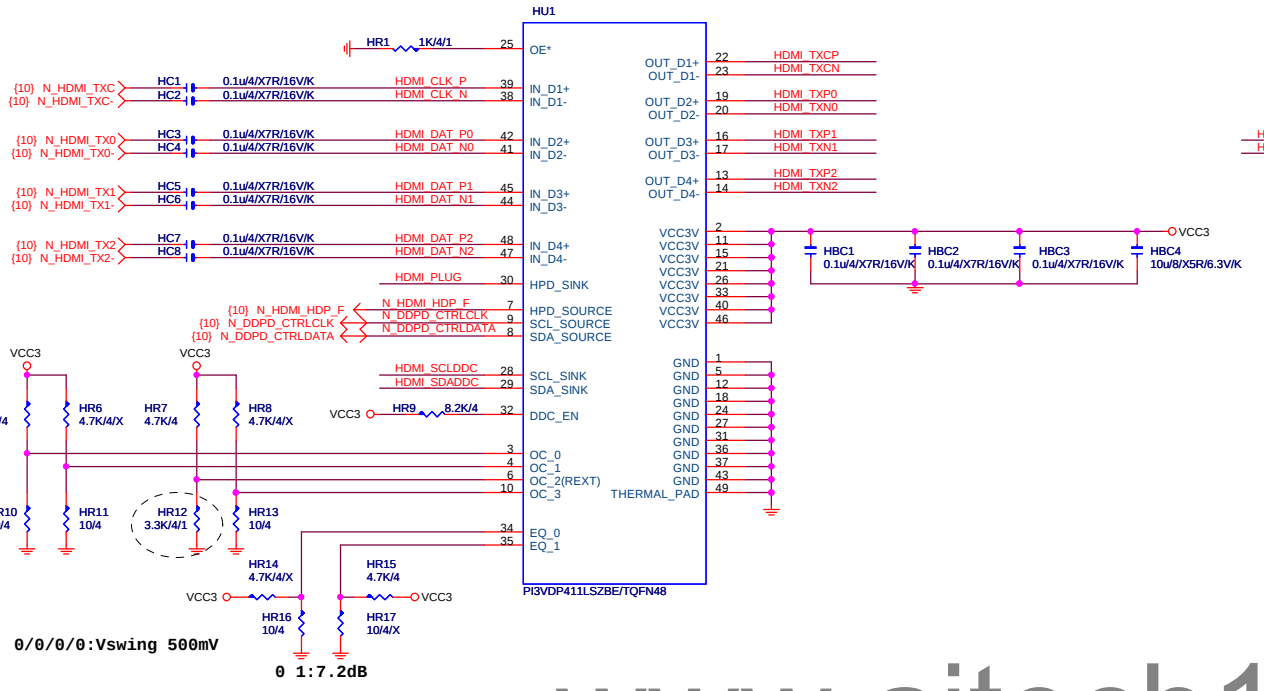

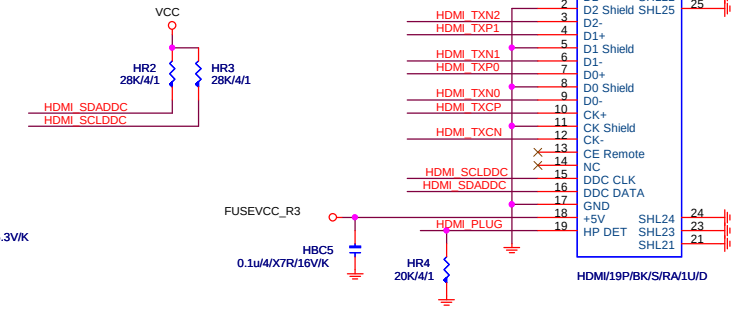

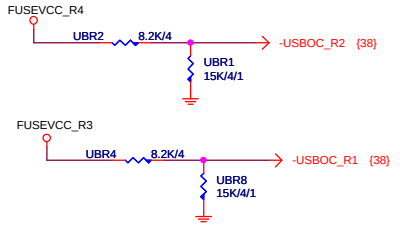

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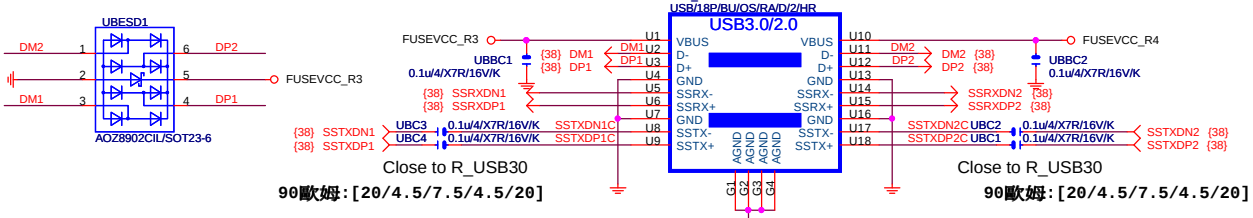

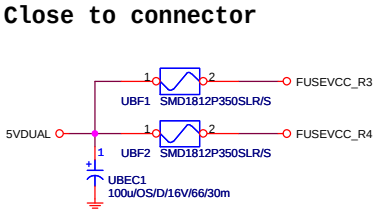

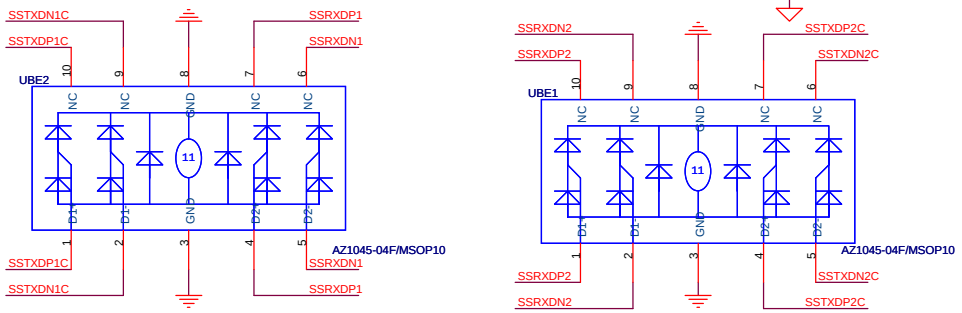

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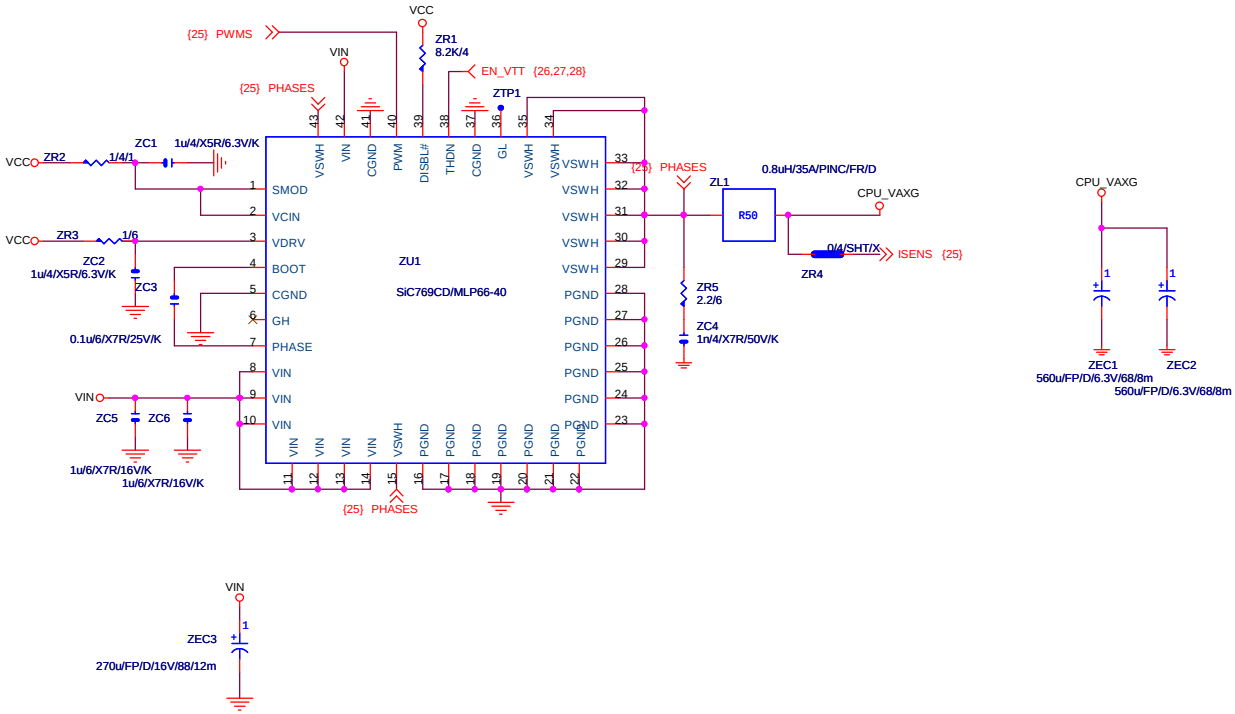

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